# INTERNATIONAL TEST CONFERENCE INDIA 2020

**JUL 12-14, 2020 | Radisson Blu, Bengaluru, INDIA**

INDIA

## Call for Papers

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. At ITC India, design, test, and yield professionals can confront challenges faced by the industry, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers. This ITC India conference will be focusing on Test development in India but the submissions may not be limited to topics related to this region. Topics related to design and test development across multi geographical regions will be of special interest.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. In addition, authors are invited to submit high quality, practical, industry best practices. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

### Submission Guidelines:

- One or two topic(s) from the topic list, or a description of your topic.
- An abstract of 35 words or less to be entered online.
- An electronic copy of a complete paper up to 10 pages or an extended summary up to 6 pages, double-columned in IEEE Format (Paper template). Submissions less than 4 pages are rarely accepted.
- Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person

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| **Abstract deadline** | **\| 08 Dec, 2019** |
| **Paper submission deadline** | **\| 05 Jan, 2020** |
| **Author notification** | **\| 15 Mar, 2020** |
| **Final manuscript due** | **\| 03 May, 2020** |

Authors are also invited to submit a single-page poster proposal, double-columned in Format (template available in EasyChair). Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper.

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| **Poster submission deadline** | **\| 18 Mar, 2020** |
| **Author notification** | **\| 15 Apr, 2020** |

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC India web site at **http://www.itctestweekindia.org** or email the program chair at itc-india-tpc@googlegroups.com

**Sponsors** (approval pending)

*ITC India invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems.*

### *Topics of interest include*

*(not limited to):*

- 3D/2.5D Test
- Adaptive Test in Practice
- ATE/Probe Card Design
- Advances in Boundary Scan
- Bring Up
- Data Driven Methods
- Data Exchange and Infrastructure
- Defect-Oriented Testing
- DFM and Test Diagnosis
- Economics of Test
- End-to-End Data Analysis
- Embedded BIST & DFT
- Emerging Defect Mechanisms
- Hardware Security and Trust
- IoT Testing
- Known-Good-Die testing
- Memory Test and Repair
- MEMS Testing
- Mixed-Signal and Analog Test
- New Technologies and Test
- On-Chip Test Compression
- Online Test
- Pre- and Post- Silicon Validation
- Power Issues in Test
- Protocol-aware Test
- Reliability and Resilience
- Scan Based Test
- SoC/SiP/NoC Test
- Silicon Debug
- Jitter, High-Speed I/O and RF Test
- Simulation and Test
- System Test (Applications)
- System Test (Hardware/Software)
- Test-to-Design Feedback
- Test Escape Analysis
- Test Flow Optimizations
- Test Generation and Validation
- Test Resource Partitioning
- Test Standards
- Test Time Analysis and Reduction
- Testing High Speed Optics/Photonics
- Timing Test
- Yield Analysis and Optimization

### *Program Co-Chairs:*

- Prakash Narayanan (Texas Instruments)
- Venkata Totakura (Cypress Semiconductor)

IEEE ttc IEEE Bangalore Section