8th IEEE International Test Conference, India
July 21-23, 2024
Radisson Blu, ORR, Bengaluru

Tutorials

Sunday, July 21, 2024

8:00am-9:30am	REGISTRATIONS		
TRACKS	TRACK 1 Session Chair | Prof. Jayagowri	TRACK 2 Session Chair | Lakshmanan Balasubramanian	TRACK 3 Session Chair | Bharath Nandakumar
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
9:30 am - 11:00 am (15 mins. Break) 11:15 am - 12:45 pm	Architecture & Methodology for DFT of Low Power SoCs Jais Abraham, Palkesh Jain, Nikhil Patil and Subhadip Kundu Qualcomm	Functional Safety Readiness: Requirements in Design, Test and Application Prasanth Viswanathan Pillai and Rubin Parekhji Texas Instruments	Optimal Scan Bandwidth Management and Structural Test Over High-Speed functional interfaces using Advanced Test Technologies Mohan Selvam, (MediaTek), Pooja Vishwanath (Synopsys), Greeshma Jayakumar (Synopsys), and Sri Ganta (Synopsys)
12:45pm-1:45pm	LUNCH BREAK		
1:45 pm - 3:15 pm (15 mins. Break) 3:30 pm - 5:00 pm	Ensuring robust RTL for DFT: Comprehensive verification strategy Parth Kadiya, Piyushkumar Chaniyara, Mahipal Reddy, Satish Sajjanar and Pervez Garg Texas Instruments DFT Designer's Nightmare in the Nanometer Age Ankush Srivastava (Qualcomm) and Kamlesh Pandey (Krivya Semicon)	Addressing Test, Safety and Security for Connected Automotive IC's Lee Harrison Siemens EDA Effective Low-Cost Strategies for Detecting Recycled Integrated circuits Ujjwal Guin Auburn University	Fault Modeling in Digital Integrated Circuits: How It Influences ATPG and DfT Bhargab B. Bhattacharya and Susmita Sur-Kolay Indian Statistical Institute, Kolkata Synchronous Interface Test Challenges for Complex ASIC, Practical Solutions for At-Speed Test Veerabhadrarao Vasa and Vevekanenda G Google

Conference

Monday, July 22, 2024

8:00am-9:15am	REGISTRATIONS		
9:00am-9:25am	Inauguration/Welcome | Sameer Chillarige, General Co-Chair, ITC India 2024		
9:25am-9:30am	Special Guest Talk		
9:30am-10:15am	Keynote: "Evolution of Semiconductor Test – Going beyond traditional production screening", Sundarrajan Subramanian – VP Engineering, Design Management , Qualcomm		
10:15am-11:00am	Keynote: "In the Decade of AI, Expectations from the DFT Community: An Outsider's Perspective", Subash Chandar Govindarajan, Senior Director, Google Silicon, India.		
11:00am-11:30am	TEA/COFFEE BREAK SESSION		
SESSIONS	Session 1: In-Field Testing Session Chair | Sneha Revankar	Session 2: Advancements in ATPG Session Chair | Sunjiv Sachan	Session 3: DFT & Reliability Session Chair | Prof. Bhargab B. Bhattacharya
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	Test Selection for Periodic In-field health-check monitoring in fail-safe applications, Ravikumar CP Concurrent Low Power Built-in Self-Test for Safety Critical SoCs Nitesh Mishra, Jemin Mehta, Hrithik Sahni and Ayushi Dixit DSP-based Mutual Testing for Automotive and Industrial ICs, Ravikumar CP	An FPGA based Emulation of Source Synchronous Protocol-Aware Timing Stress Test, P R R K Tirumalesu Manda, Vinodh J Rakesh, Vasavi Ghanta and Jagadish Raju Krishna Raju Optimize Test Pattern Count via Efficient Operation of IEEE 1687 SIBs, Divyank Mittal, Rajesh Khurana and Akanksha Bansal Optimized Timing Aware ATPG for At-Speed Test of Cell Internal Faults, Aneri Jain, Wilson Pradeep and Andreas Glowatz	A Hybrid Test Point Insertion Strategy for Improved Test Metrics, Nikita Naresh, Naushad Ali, Krunal Siddhapathak, Wilson Pradeep, Nilanjan Mukherjee, Oussama Laouamri and Karthick Prabhu D Shift Power Reduction in High-Performance Clock Network Designs, Kamlesh Bhesaniya, Omar Sharif Cherukur, Lakshmi Kandula, Ravishankar Chevuri, Pradeep Sreenivasa and Anoop Padmanabhan Exploring Cross-Temperature Reliability in 3D NAND Through Layer-dependent Bit Error Analysis, Anik Kumar Mondol and Biswajit Ray
01:00pm-2:00pm	LUNCH BREAK		
HALL NAME	GRAND VICTORIA		
2:00pm-2:45pm	Invited Talk: "Test Challenges in AI and Chiplet Era", Rajesh Vaddempudi, Tessolve		
2:45pm-3:30pm	Keynote: "From chip to system – The expanding world of test", Lee Harrison, Siemens		
3:30pm-4:00pm	TEA/COFFEE BREAK SESSION		
SESSIONS	Panel Discussion Session Chair | Kamlesh Pandey		Poster Session Session Chair | Pranjal Giri

HALL NAME	GRAND VICTORIA	ARABICA & ROBUSTA
4:00pm-5:30pm	The role of AI in improving EDA tools and SOC test methodologies: Opportunities and Challenges Panelists: Prakash Narayan (Google) Krishna Chakravadhanula (Cadence) Navin Bishnoi (Marvell) Ruchir Dixit (Siemens) Chandan Kumar (Synopsys)	Poster Session

Tuesday, July 23, 2024

8:30am-9:15am	REGISTRATIONS		
9:15am-9:30am	Welcome / Day 2 Summary | Venkata Rangam Totakura, General Co-Chair, ITC India 2024		
9:30am-10:15am	Keynote: "Fault-Criticality Classification and Test Solutions for Systolic Array-Based AI Hardware", Prof. Krishnendu Chakrabarty, Arizona State University		
10:15am-11:00 am	Keynote: "Accelerated Compute's Impact on Test Development", Bill Cornwell - AVP, CCS (Custom, Compute & Storage) DFT , Marvell		
11:00am-11:30am	TEA/COFFEE BREAK SESSION		
SESSIONS	Session 4: Analog & Mixed Signal Test Session Chair | Dundapa Sankpal	Session 5: Emerging Technologies & Applications Session Chair | Vikram Kuralla	Session 6: Verification & Validation Methodologies Session Chair | Prakash Talawar
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	Application Specific Integrated Data Processing in ADCs for High Accuracy, Low Latency Advanced Real Time Control, Systems Varshashree Kottadamane, Prasanth Viswanathan Pillai and Ibukun Olumuyiwa Shift-Left Principle for Faster Post-Silicon Validation: LPDDR4 Controller Bring-up, Vinodh J Rakesh, Jithesh Pothandy Karayi, Chaitanya Kumar Reddy Mallu, Karthick Somu, Vasavi Ghanta and Timmy E Peter Silicon correlation in SLM: An Integrated Strategy for Chip performance optimization, Abhishek Das, Durga Prasad Bade, Leela Krishna Thota and Akshay Kavukuntla	On the Asymmetry of Stuck-at Fault Sensitivity in Memristive Neural Architectures, Manobendra Nath Mondal, Animesh Basak Chowdhury, Santlal Prajapati, Susmita Sur-Kolay and Bhargab B. Bhattacharya Application of Machine Learning in De-embedding of Signal Integrity Parameters for High Speed Serial Link, Maneesh Pandey, Mohit Goyal and Ajay Dash In-field fault detection framework for Edge Accelerator using Autoencoder, R S Haripriya and Jaynarayan T Tudu	LLM Assisted Assertion Generation for RTL Design Verification, Bhabesh Mali, Maddala Karthik and Chandan Karfa A Formal Based Verification Methodology for DFD Mux-Tree Hierarchies, Maneesh Pandey, Madhav Lekkala, Nikhitha Chintagumpala, Bhagyaakshmi C and Surya Ramasamy Accelerating First Silicon Validation By Leveraging FPGA Capabilities, Jenish J Palathingal, Deepu K Krishnan, Sreeram V. R. and Divya D.S.
01:00pm-2:00pm	LUNCH BREAK		
SESSIONS	Industry Session - 1 Session Chair | Sandeep Jain	Industry Session - 2 Session Chair | Mehala Balasundaram	TRC Session Chair | Leela Thota
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2:00pm-3:30pm	Navigating the complexities of test engineering, Mudasir Kawoosa, TI 1687 Standard Extensions, Prasad Mantri, Eximietas Design Expedite time to market by optimizing the test program development cycle time using AI/ML algorithms, utilizing synthetic data generation, Kalyana Sundaram Chandran, Caliber Interconnects	Hierarchical Low Toggle ATPG, Ankush Srivastava, Qualcomm Targeting bridges and opens with physical defect-based approach, Suraj M C, Marvell Innovative Testing Strategies for the Future of Semiconductor Testing, Shitendra Bhattacharya, Emerson (formerly NI)	HTOL Controller –A Next Gen Stress methodology Coverage analysis, Boopala Krishnan Synchronization of Master-Slave Embedded TAP controllers for IEEE 1687 based design configurations, Sagar Kumar, Divyank Mittal, Rajesh Khurana and Akanksha Bansal Test Method and Apparatus for Additive Jitter Correction in Mesh based Clock Architectures, Sudheer Anumala, Sri Sakthi Santhanam and Ankita Dhole, Intel Design and Development of In-Memory-Compute SRAM cell using 45nm Technology, Usha Mehta and Shubham Thaker
3:30pm-4:00pm	TEA/COFFEE BREAK SESSION		
SESSIONS	Industry Session - 3 Session Chair | Shamitha Rao		
HALL NAME	GRAND VICTORIA		
4:00pm-5:30pm	DFT and Silicon Health Optimization with AI driven test and Silicon Life Cycle Management, Mohammed Hussain, Synopsys Advances in a Shift-Left strategy for DFT, Nilanjan Mukherjee, Siemens Advancing Trustworthy Automotive Semiconductor Designs: Leveraging Modus and Midas, Pradeep Nagaraj, Cadence		
5:30pm-5:45pm	Closing Ceremony		