23-25 JULY, 2023
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7th IEEE

International Test Conference India 2023

Proceedings

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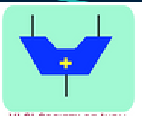

Message from General Chair

Sameer Chillarige

Cadence

The semiconductor test domain is becoming an increasingly challenging and exciting space for the engineering and research communities.

In a span of three decades, test has transformed from an optional technology to a mission-critical technology; test has expanded its wings to every step from design inception to post-silicon; test automation has become an intelligent hardware/software collaboration problem from a computationally hard software problem; and ideas from test are effectively getting extended to the security and reliability domains. Test economics has been an interesting space for those who seek insights, and it is becoming much more exciting with test becoming a part of the silicon lifecycle.

On the other hand, Governments across the globe are enabling more innovation in the semiconductor space through various policies and programs. There is a never-before-seen push from the Indian Government to kickstart semiconductor manufacturing and assembly, where testing plays a vital role. In light of these developments, it is imperative for the niche semiconductor test community to stay connected with the ongoing research and advancements in the test domain. The ITC India conference is one such platform to connect, learn, and share information. The conference, which started in 2017 with the intent to connect and build a test community in the India region, has garnered tremendous strength and support with each edition. Through this platform, many workshops and seminars are conducted throughout the year at the premier institutes in the country to talk about semiconductor testing. Thanks to the sponsors and supporters, a number of fellowships are offered to academics to participate in the conference and stay connected with the industry.

The 7th edition of ITC India is going to happen from July 23rd-25th at Radisson Blu, ORR, Bengaluru. The technical agenda is prepared with extreme care to cover the breadth of topics and spectrum of attendees. We will be kick-starting this edition with 10 Tutorials on topics ranging from the basics to contemporary topics in DFT, Test, and Security. In the subsequent two days, there are four exciting keynotes planned on emerging topics such as Silent Data Corruption (SDC), Silicon Life Cycle Management (SLM), Analog Test, Test challenges in full flow, and time-to-closure. Due to the significantly higher number of paper submissions this year, we ended up selecting more research papers and will be running three parallel tracks for paper presentations as opposed to two tracks in previous editions. The program is not just filled with engaging presentations, panel discussions from industry veterans and academicians but also includes a number of poster presentations from enthusiastic engineering community.

Message from General Chair

Kamlesh Pandey

Qualcomm

A very warm greeting to one and all. I am sure you all will be very excited to participate in 7th edition of ITC India scheduled to start from July 23. The ITC India organizing committee has diligently put together very diversified and technically rich program for 3 days. The VLSI test domain continues to grow and keep expanding its footprint in silicon product life cycle. Modern SOCs are making huge inroads into mission critical applications such as automotive, industrial automation, and health care systems that demand high quality and reliability. The mission critical applications not only require high defect coverage for final testing but also need capabilities to continuously perform self-test, monitor and analyze latent, environmental, and aging induced random defects that can cause fatal failures and accidents. This requirement is driving growth of silicon life cycle management (SLM) faculty.

To proliferate test at grassroot level, we are looking forward to seeing greater participation from student and faculty communities from academia domain. The test is a very exciting faculty of chip design process as it starts from chip architecture phase and goes all the way till end of the chip lifetime. The test directly affects profitability and brand image. It gives immense pleasure and deep sense of fulfillment when extremely tricky silicon problems related to Vmin, Fmax, power, yield fall out, test escapes and shmoo holes are root caused using extremely cryptic and limited fail signatures. Sometimes these problems are extremely difficult to reproduce in simulations/emulations and cannot be observed or controlled directly on tester.

I firmly believe that ITC is a mega festival for test diehard fans and provides an excellent opportunity to receive and give peer reviews and feedback on key test issues to fellow test engineers.

The semiconductor test domain is becoming an increasingly challenging and exciting space for the engineering and research communities.

Message from Technical Program Chairs

Venkata Rangam Totakura
Infineon

Kavitha Shankar
Marvell Semiconductor

Prof. S. Sivanantham
VIT, India

Prof. Priyank Kalla
The University of Utah, USA

Welcome to the 2023 IEEE International Test Conference India (ITC-India), the 7th in a series of events that explores emerging trends, innovative research and scalable solutions to the challenging problems of electronic test of devices, boards and systems. The two-day technical program includes exciting sessions covering research and applications on emerging topics such as Artificial Intelligence and Machine Learning in Test, Hardware Security in Test, Power-aware DFT and Functional Test, as well as advancements in core Validation and Test methods, MBIST Test, Diagnosis and Analog/RF Test.

ITC-India is a truly international event. The technical program committee (TPC) received 123 paper submissions from 10 countries. The TPC comprising around 80 members from both industry and academia thoroughly reviewed the submissions, where each submission received at least 4 reviews. The final program was selected by the TPC to include 21 high quality papers covering the entire gamut of Test and Design-for-Test (DFT) related topics. The program further includes an exciting panel discussion on Voltage bump decisions during test application. Moreover, a session is organized with two invited presentations on hot-topics of Circuit Timing Marginalities and Robustness Evaluation in complex SoCs. As is the norm, ITC-India program also includes the traditional Test Reality Check and Academia Research Tracks.

This year, ITC-India has invited four speakers from academia and industry to present four keynote talks that pose intriguing questions on using Structural Test for Silent Data Errors or for Analog/RF Test, as well as cover Disruptive Technologies and corresponding Test Solutions. The TPC expresses their gratitude to the keynote speakers, who are leaders in their respective fields, for sharing their vision and experience with the attendees.

The ITC-India technical program is the result of the volunteer efforts of more than 30 dedicated researchers and professionals. The TPC members have particularly made significant contributions to ensure a high-quality program. The TPC chairs thank them for their efforts. The goal of ITC-India committees is to bring a program covering upcoming and future test challenges to meet your evolving needs, as well as contemporary challenges faced by the test community. Please take the opportunity during the meeting to let us know how we can do this better. We welcome your comments and suggestions.

ITC-India is your conference. We encourage you to actively participate in it. The TPC chairs hope that as a result of your lively interaction, you will find ITC-India 2023 interesting, valuable and fun!

ITC India 2023 Committee

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Kamlesh Pandey, Qualcomm India Pvt Ltd

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Kavitha Shankar, Marvell Semiconductors India
Prof. Sivanantham, VIT, Vellore
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Tutorial Program

Sunday | July 23, 2023

Sunday, July 23, 2023			
8:00am-9:30am	REGISTRATIONS		
TRACKS	TRACK 1 Session Chair | Santosh Kumar	TRACK 2 Session Chair | Dr. Subhadip Kundu, Krishnamachary Prathapuram	TRACK 3 Session Chair | Prof. R. Jayagowri
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
9:30 am - 11:00 am (15 mins. Break) 11:15 am - 12:45 pm	Seamless Integration of packetized scan with Advanced ATE equipment **Lee Harrison (Siemens), Peter Orlando (Siemens), Michael Braun (Advantest) and Pudhukkarai Krishnan (Advantest)**	Design for Test – An indispensable slice of SOC (System on Chip) life cycle **Shamitha Rao, Bala Krishna K (Intel)**	DFX beyond Compression **Vijay Kumar K S, Kranthi Kandula, Leela Krishna Thota and Paras Chhabra (Synopsys)**
12:45pm-1:45pm	LUNCH BREAK		
1:45 pm - 3:15 pm (15 mins. Break) 3:30 pm - 5:00 pm	Error Resilient AI System: Addressing Soft Errors, Security, Threats and Manufacturing Variability Effects **Prof. Abhijit Chatterjee (Georgia Tech, USA)** Guaranteeing quality in automotive EMC tests through in-house EMC test **George Thottan, Rajesh Chauhan and Dilip Jain (Texas Instruments)**	Power Domains and Physical Synthesis – A DFT Perspective **Sarthak Singhal, Subhasish Mukherjee, Dr. Krishna Chakravadhanula and Bharath Nandakumar (Cadence)** Hierarchical and tile based DFT techniques for AI and Large SoCs **Lee Harrison and Peter Orlando (Siemens)**	Hardware Security: A perspective towards Fault Analysis Vulnerabilities **Prof. Bodhisatwa Mazumdar (IIT Indore)** Power Aware DFT **Karthik Natarajan, Likith Manchukonda, Manish Arora, Rahul Singhal and Greeshma Jayakumar (Synopsys)**

Conference Agenda

Day 1 | Monday | July 24, 2023

Monday, July 24, 2023			
8:00am-9:15am	REGISTRATIONS		
9:00am-9:25am	Inauguration/Welcome | Sameer Chillarige, General Co-Chair, ITC India 2023		
9:25am-9:30am	Special Guest Talk | Srinivas Chinamilli, CEO, Tessolve		
9:30am-10:15am	**Keynote:** "Can Structural Test play a role in mitigating Silent Data Errors?", Dr. Nilanjan Mukherjee, Siemens		
10:15am-11:00am	**Keynote:** "Test industry challenges and solutions as observed by the leading physical implementation solution provider", Janet Olson, Cadence		
11:00am-11:30am	TEA/COFFEE BREAK SESSION		
SESSIONS	Session 1 MBIST Test Challenges Session Chair | Sandeep Jain	Session 2 Productivity Enhancement through Improved Diagnosis Session Chair | Veejaye Panayadian	Session 3 AI/ML in Test Session Chair | Jyotirmoy Saikia
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	1.1. Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation, Nikhil Karkare and Wilson Pradeep 1.2 MBIST-HSIO Concurrent Testing Strategies and Test Challenges, Boopala Krishnan, Shalini Mishra, Sumit Emekar, Subrahmanya M, Prasanna Ramanujam, Melvin Cu and Linfeng Pu 1.3 MBIST Area & Test Time Optimization Using Machine Learning Techniques, Darakshan Jamal and Ratheesh Thekke	2.1 A novel test data compaction method with improved debug capabilities of the signatures, Jaidev Shenoy, Kelly Ockunzzi and Dr. Virendra Singh 2.2 A novel approach to identifying scan issues during RTL validation, Alli Sravan, Malagiri Shashi Vardhan Reddy, Velamala Nithin and Ravathkar Ashwin Kumar 2.3 Addressing physically aware diagnosis challenges in hierarchical core based designs, Bharath Nandakumar, Sameer Chillarige, Robert C Redburn, Jeff Zimmerman and Nicholai L'Esperance	3.1 Application of Machine Learning in De-embedding of Signal Integrity Parameters for High Speed Serial Link, Maneesh Pandey, Mohit Goyal and Ajay Dash 3.2 Machine Learning Based MBIST Area Estimation, Puneet Arora, Virad Jain, Tarun Goyal and Norman Card 3.3 Hardware Simulator : Virtual Testing and Non-Product Failure Isolation, Akhila K, Shalini Srinivasan N, Gopikrishnan K and Harish G L
01:00pm-2:00pm	LUNCH BREAK		
SESSIONS	Industry Session - 1 Session Chair | Shamitha Rao		ART Session Chair | Prof. Usha Mehta, Sandeep Jain
HALL NAME	GRAND VICTORIA		ARABICA & ROBUSTA
2:00pm-3:30pm	1. "Test Challenges in Known Good Die Chiplets based heterogeneous integration", Yogan Senthilkumar, Tessolve 2. "Advancements in Mixed-Signal Testing and Verification using Analog DFT Techniques", Prasanna Ramanujam, Qualcomm 3. "Silicon Life Cycle Management", Santosh Kumar, Synopsys		ART 1.1. Quality metric based optimal test option generation for small delay defects, M Prathiba and S Sivanantham ART 1.2. Lightweight Secured Split Test Technique with RMA Capability for Integrated Circuits, Sudeendra Kumar K, Akshay Girish Kaushik, Adithya B Shetty, Ashutosh Rao and Akshay S ART 1.3. Detection of hardware Trojans using Decision Tree Classifier at RTL of an ICs present in IoTs, Lavanya T and Dr Rajalakshmi K
3:30pm-4:00pm	TEA/COFFEE BREAK SESSION		
SESSIONS	Panel Discussion Session Chair | Kamlesh Pandey		Poster Session Session Chair | Bharath Nandakumar, Pranjal Giri
HALL NAME	GRAND VICTORIA		ARABICA & ROBUSTA
4:00pm-5:30pm	Voltage bump decisions to work around Vmin issues: are these based on any science or pure tribal art? 1.Jais Abraham (Qualcomm) 2.Srinivas Vooka (Google) 3.Prasad Mantri (AISemiCon) 4.Steve Palosh (Cadence) 5. Malav Shah (TI)		Posters

Conference Agenda

Day 2 | Tuesday | July 25, 2023

Tuesday, July 25, 2023			
8:30am-9:15am	REGISTRATIONS		
9:15am-9:30am	Welcome / Day 2 Summary | Kamlesh Pandey, General Co-Chair, ITC India 2023		
9:30am-10:15am	**Keynote:** "Disruptive Technologies Drive a New Era of Test", Dr. Faadi Maamari, Synopsys		
10:15am-11:00 am	**Keynote:** "Paradigm Shift: Structural Approaches to Analog and RF Test", Prof. Sule Ozev, Arizona State University		
11:00am-11:30am	TEA/COFFEE BREAK SESSION		
SESSIONS	Session 4 Power Aware DFT & Functional Test Session Chair | Raghu GG	Session 5 Advances in security Session Chair | Prof. Priyank Kalla	Session 6 Validation & Test Methodologies Session Chair | Balaji Upputuri
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	4.1 Power Domain Aware DFT Implementation, Sarthak Singhal, Subhasish Mukherjee, Christos Papameletis, Krishna Chakravadhanula, Ankit Bandejia, Dale Meehl, Archana Vyas and Mohan Gandla 4.2 Design of a Fault-Tolerant Pseudo-3D Routing, Biswajit R Bhowmik and Gagan N 4.3 Parallel Functional Test : A case study to reduce test cost in large SOCs, Akshatha P Inamdar, Syed Shadab and Karthik Chandrashekar	5.1 Invisible Scan for Protecting against Scan-based Attacks: You Can't Attack What You Can't See, Pravin Gaikwad, Patanjali Slpsk and Swarup Bhunia 5.2 Hidden in Plain Sight: A Detailed Investigation of Selectively Increasing Local Density to Camouflage and Robustify Against Optical Probing Attacks, Sajjad Parvin, Chandan Kumar Jha, Sallar Ahmadi-Pour, Frank Sill Torres and Rolf Drechsler 5.3 PROTECTS: Secure Provisioning of System-on-Chip Assets in Untrusted Testing Facility, Patanjali Slpsk, Jonathan Cruz, Sandip Ray and Swarup Bhunia	6.1 Scalable and Comprehensive approach for Concurrency Validation to improve Platform Stability, Naveena Nataraj, Jayaprakash Bs, Chockalingam A, Mandira Kumar Sathanantham, Kishore Chittudi, Ravishankar S, Abhishek Paliwal and Nihar Ranjan Saha 6.2 A formal approach to improve connectivity coverage in DFD, DFT, DFM, and DFX domain, Jayashri Patil, Kruttika Golwelker, Manu Yeeshu, Sood Surinder, Ananth Deepak K. S. and Shruti Deshpande 6.3 Prevention of High Current Events during Hot Testing at Turbo Frequency, Navaneeth A, Tiwari Himanshu, Sankapal Dudapa B and Vetcha Anand S
01:00pm-2:00pm	LUNCH BREAK		
SESSIONS	Industry Session - 2 Session Chair | Shamitha Rao		Session 7 Overcoming Analog/Mixed-Signal Test Challenges Session Chair | Prof. Sivanantham
HALL NAME	GRAND VICTORIA		ARABICA & ROBUSTA
2:00pm-3:30pm	1. "SSN - the next big thing", Lee Harrison, Siemens 2. "Mixed Signal Test - Challenges and Solutions", Nagarajan Viswanathan, Texas Instruments 3. Innovus Test Point - Enabling the next leap in coverage and test pattern reduction, Steve Palosh, Cadence		7.1 Analysis of Non-idealities in On-chip Loopback Testing of Data Converters, Tamajeet Mandal, Aswin R and Rubin Parekhji 7.2 Unified Analog Mixed-Signal Defect Simulation and Applications, Krishna Kumar Ganapathy Raman, Aswin R, Arshad Qureshi, Supraja R, Chanakya K V, Vijay Kumar Sankaran, Vinay Rawat, Victor Zhuk and Lakshmanan Balasubramanian 7.3 An SoC based Cost Effective Static Linearity Test Scheme for ADCs, P R R K Tirumalesu Manda and Keerthan Rai
3:30pm-4:00pm	TEA/COFFEE BREAK SESSION		
SESSIONS	Invited Talks Session Chair | Venkatarangam Totakura, Kavitha Shankar		Test Reality Check Session Chair | Vishal Vadhavania, Dimple Aggarwal
HALL NAME	GRAND VICTORIA - A		ARABICA & ROBUSTA
4:00pm-5:30pm	1. Circuit Timing Marginalities and Silent Data Corruption, Prof. Adit Singh, Auburn University 2. Methodologies to evaluate Robustness of Modern Complex SoCs, Dr. Surya Musunuri, Infineon		TRC 1.1 HTOL Vector Utility(VecUtil) Tool For Protocol Aware Vectors, Boopala Krishnan, Shalini Mishra, Prasanna Ramanujam and Subrahmanya M TRC 1.2 Curious Case of Fab Process Variation on PLL Lock, Ajmal Firdous, Syed Feruz Syed Farooq, Himanshu Tiwari, Govil Badghare, Rucha Rathi and Kishore Kumar Banda TRC 1.3 Design/Manufacturing Challenges & Solution for highly Dense and large ATE DUT Boards, Rajiv Vk TRC 1.4 Novel Methodology to Optimize TAT and Resource utilization for ATPG Simulations for Large SoCs, Sudhakar Kongala, Anuj Gupta, Yash Walia and Sahil Jain
5:30pm-5:45pm	Closing Ceremony		

Tutorial 1

The Seamless Integration of Packetized scan with Advanced ATE Equipment

Sunday July 23, 2023

Tutorial Summary:
This tutorial, will cover the basics of packetized ATPG data, including the hardware generation, configuration, pattern generation and ATE program creation. Detailing how this is seamlessly integrated with ATE equipment to support functions such as data logging and diagnostics.

Lee Harrison is Product Marketing Director, with the Tessent product division at Siemens EDA. He has over 20 years of industry experience with Mentor DFT products and has been involved in the specification of new test features and methodologies for Mentor customers, delivering high quality DFT solutions. With a focus on Automotive, Lee is working to ensure that current and future DFT requirements of Mentor's Automotive customers are understood and met. Lee Received his BEng in MicroElectronic Engineering from Brunel University London in 1996. Lee presents regularly at industry conferences such as DAC, ITC, VTS, ETS, DATE etc.

Peter Orlando is the SSN Product manager and part of the Siemens Tessent DFT Product Marketing team. Since joining Siemens 2018, Peter has been part of the development of SSN product and primarily responsible of the deployment of SSN. As the customer facing technical lead for the SSN product, Pete has been providing implementation guidance to external customers and internal colleagues. He's been part of many designs that have successfully taped out with SSN. Pete's role in SSN continues to expand with the development and deployment of new features being added to regularly.

Pudhukkarai Krishnan is a Solution Architect with Advantest R&D focusing on the 93000 Tester platform. He has been in the Semiconductor Test field for more than 25 years working in various roles like applications engineering, product definition and validation, focusing on digit al and high-speed memory test areas.

Michael Braun is a Product Marketing Manager for Semi-Conductor test at Advantest

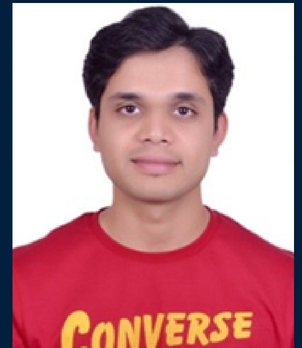
Tutorial 2

DFX beyond Compression

Sunday July 23, 2023

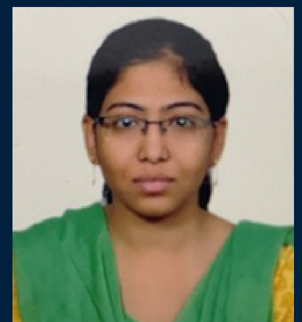
Tutorial Summary:
As the advancements on the technology is mounting, the evolution of application space led the requirements of increased performance, cost reduction, faster time to market, reliability, and functionality of the chips, making designs enormous & complex. Due to the rapid growth in semiconductor market, methodologies like multi-core design, chiplets, system-on-chip (SoC) design are proposed to squeeze out every bit of performance and meet aggressive time to market goals.

Vijay Kumar K S is a Staff Solutions Engineer at Synopsys. He began his career at Texas Instruments and worked for SiCon Design Technologies and Nvidia before joining Synopsys. He has around 14 years of experience in VLSI industry working on Design for Testability (DFT). He has worked extensively on DFT implementation on multiple SoCs. Vijay's current focus is development and deployment of Automotive DFT solutions. He leads a team of engineers working on cutting-edge DFx solutions.



Leela Krishna Thota Currently working in Synopsys as Senior Solutions Engineer II, Silicon Realisation group, Hardware Analytics Team. Current work focus is on Silicon LifeCycle Management & Streaming Fabric. Overall VLSI experience is 9+ years in a collateral production role at various companies that includes the exciting work involved with Samsung Semiconductor India Research & Development(Foundry design services), Altran & SiCon Design Technologies Pvt. Ltd. Besides DFT, gained VLSI board design knowledge in Wipro.

Kranthi Kandula is a R&D Manager in Hardware Design Group in Synopsys. Currently Managing Digital Design and DFT team in Synopsys for SLM (Silicon Lifecycle Management), Test and Debug IP's. Prior to joining Synopsys she has worked at AMD in SOC DFx Validation.She has around 8 yrs of experience in VLSI industry and has worked extensively in designing, development, and validation of new DFx solutions.



Paras Chhabra is a Senior Manager in Hardware Analytics and Test group of Synopsys, responsible for Hierarchical Test and Pattern Management. He joined Synopsys in 2019 from Nvidia Graphics. He has also worked with Cadence Design Systems and Mentor Graphics. Paras has a B.Tech. (H) in Electronics and Electrical Communication engineering from IIT Kharagpur, batch of 2001. He also has an M.Tech. in VLSI Design Tools and Technology from IIT Delhi.

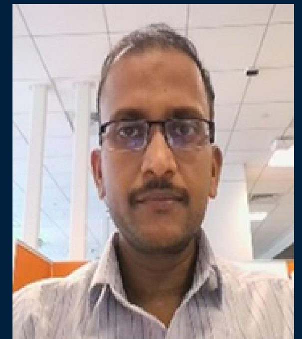
Tutorial 3

Design for Test – An indispensable slice of SOC (System on Chip) life cycle

Sunday July 23, 2023

Tutorial Summary:
The objective of this tutorial is to provide valuable information and make a conscious attempt to explain the basic concepts of Design For Test (DFT) through examples and illustrations. This tutorial also helps to map theoretical DFT knowledge gained from academics to the actual DFT application during various phases of SoC development and life cycle. This tutorial aims to focus on introducing various DFT techniques and implementation methods used in System On Chip(SoC) Life Cycle with emphasis on the popular methods used for digital logic and memory testing. This includes explaining DFT techniques used to screen various defects on Silicon before shipping to the customer, as well details of design infrastructure required for enabling the same. We will also provide insights to various nonstandard techniques that are used for special components in SOC like IOs/Analog etc. We will take a glance at special requirements for Automotive SoCs. In conclusion, we will introduce to Design for test techniques for yield improvement and debug that is used in the industry.

Bala Krishna K is currently working as a Technical Lead Engineer at Intel India Pvt Ltd. He completed his Bachelors in Electronics at NIT, Warangal and Masters in Microelectronics at Manipal University. He has around 18 years of VLSI industry experience with an expertise on Design-For-Test domain for complex sub-systems and System-On-Chips across process nodes. He was involved in end-to-end industry standard DFT activities that include Architecture, Implementation, support to the Silicon screening on Automated Test Equipment and debugging of post silicon customer returns.



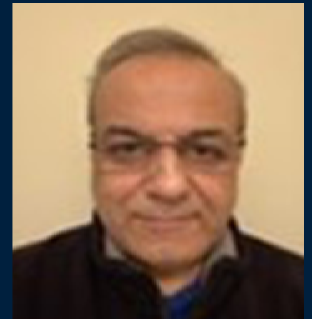
Shamitha Rao is SOC Design Eng Manager, Design for Test in Super Computing Platform group at Intel. Shamitha is currently leading end to end DFT implementation and validation on complex SoCs while actively mentoring multiple DFT engineers to achieve excellence in DFT execution. Shamitha has over 18 years of experience in DFT, with expertise ranging from creating best in class flows for DFT implementation/validation to defining and implementing DFT solutions to cater to customer/design needs and end to end DFT execution on complex designs.

Tutorial 4

Error Resilient AI System: Addressing Soft Errors, Security, Threats and Manufacturing Variability Effects

Sunday July 23, 2023

Tutorial Summary:
The reliability of emerging neuromorphic compute fabrics is of great concern due to their widespread use in critical data-intensive applications. Ensuring such reliability is difficult due to the intensity of underlying computations (billions of parameters), errors induced by low power operation and the complex relationship between errors in computations and their effect on network performance accuracy. In this tutorial, we study the problem of designing error-resilient neuromorphic systems where errors can stem from: (a) soft errors in computation of matrix-vector multiplications and neuron activations, (b) malicious trojan and adversarial security attacks and (c) effects of manufacturing process variations on analog crossbar arrays that can affect DNN accuracy.



Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech and a Fellow of the IEEE. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Dr. Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received seven Best Paper Awards and three Best Paper Award nominations. His work on self-healing chips was featured as one of General Electric's key technical achievements in 1992 and was cited by the Wall Street Journal. In 1995, he was named a Collaborating Partner in NASA's New Millennium project.

In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. In 2007, his group received the Margarida Jacome Award for work on VIZOR: Virtually Zero Margin Adaptive RF from the Berkeley Gigascale Research Center (GSRC). Dr. Chatterjee has authored over 450 papers in refereed journals and meetings, has 22 patents and supervised over 50 Ph.D dissertations. He is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as chairman and chief scientist from 2000-2002. His research interests include error-resilient machine learning, signal processing and control systems, mixed-signal/RF/multi-GHz design and test and adaptive real-time systems.

Tutorial 5

Guaranteeing quality in automotive EMC tests through in-house EMC test

Sunday July 23, 2023

Tutorial Summary:
Automotive industry is very safety critical, as any component failure in an automobile subsystem can lead to accidents and even loss of life. Automotive electronics today is in a fast-growing trajectory and is a major market where semiconductor industry focuses its resources. Automotive electronics has unique set of problems given the solution density and harsh operating environment. This extremely competent industry subjects all electronic subsystems to extensive Electromagnetic compatibility (EMC) tests to ascertain quality and reliability. These tests are highly resource and time intensive. Current market philosophy drives to incorporate a “Design for EMC” approach to identify EMC problems upfront to address them early in the design stages to minimize cost and cycle time. This strategy requires robust EMC checks at component level prior to a subsystem or vehicle level checks. It opens up a completely new domain of tests under silicon validation for automotive IC’s. This calls for better understanding of EMC tests by validation engineers to perform quality assessment of products. This tutorial outlines firsthand how such an initiative in Silicon validation has brought out significant impact in terms of winning shares and leading the market.

George Thottan, Validation Manager, Power Switches, Analog Power Products George joined TI in 2016. He holds a Master’s degree in Electronics Design Technology. He had been the lead validation engineer across multiple automotive products across different TI portfolios like High Side controllers, Ideal diode controllers and High Side switches. He was the technical lead for a team which worked to establish an inhouse EMC set up in TII.

Rajesh Chauhan, Validation Manager, Motor Drives, Analog Signal Chain Rajesh Chauhan joined TI in 2016. He holds a Master’s degree in Communication system. He had been the lead validation engineer across multiple Industrial and Automotive products across different TI portfolios like Transceivers, Mux and Switches and Motor drives. He is currently the part of team which working to establish an inhouse component level EMC set up in TII.

Dilip Jain, Systems Manager, Power Switches, Analog Power Products Dilip Jain is responsible for roadmap development and defining products such as Ideal Diode controllers and 100V smart high side controllers. He was elected to MGTS tech ladder title in 2021. He has 14 years of broad experience in power management domain with expertise in power supply design and circuit protection for Automotive and Industrial power. He holds a master’s degree in Electrical Engineering from the Indian Institute of Technology, Bombay.

Tutorial 6

Power Domains and Physical Synthesis – A DFT Perspective

Sunday July 23, 2023

Tutorial Summary:
Power and Physical awareness has become an important dimension for recent advances in VLSI. Physical synthesis, the integration of logic synthesis with physical design information, was born in the mid to late 1990s. Fast forward to 2023, It is the de-facto implementation approach for any modern mid or large sized SoC. Unified Power Format (UPF) is the popular name of the Institute of Electrical and Electronics Engineers (IEEE) standard for specifying power intent in power optimization of electronic design automation published in 2009. Along with physical synthesis, UPF is also a must have for low power SoCs specifically for IoT and automotive applications. With increasing power demands in modern SoCs, a lot of academic & industrial research is done to design macros operating in multiple low power modes depending upon the voltage value of each supply. Multiple functional power domains (PD) are forcing Design-for-Test (DFT) designers to adjust DFT insertion and implementation to comply with IEEE 1801 correctness.

Sarthak Singhal is working as Sr. Principal Product Engineer for Modus DFT Software Solutions at Cadence Design Systems. He has over 10 years of industry experience. His focus includes DFT architectures and methodologies. He is responsible for augmenting Cadence DFT and ATPG tools by deploying, architecting and supporting new TEST methodologies and flows across customers. He has published four IEEE conference papers in India & US. He graduated from NIT, Allahabad majoring in Electronics and Communication Engineering in 2012.

Bharath Nandakumar is Principal Software Engineer in Modus DFT Software Solution R&D group at Cadence Design Systems, Noida. He manages the Diagnostics and User Interface team. His 6+ years of experience at Cadence involves working on multiple research projects to enhance the Modus software, resulting in multiple publications. He is an active member of ITC India 2022, 2023 committee. He received his Master's degree in VLSI Design Tools & Technology from Indian Institute of Technology, Delhi.

Subhasish Mukherjee is a passionate learner and has a penchant to find viable solutions to software and hardware complexities. Subhasish has been a key developer of many complex features of Cadence DFT product base. He is working as a Software Engineering Director and is leading the Cadence DFT development activities in India. He received multiple organizational awards at Cadence, holds multiple US patents, authored several papers in IEEE conferences and international journals and was session chair at different national and international VLSI and Test conferences.

Tutorial 7

Hierarchical & tile based DFT techniques for AI & Large SoCs

Sunday July 23, 2023

Tutorial Summary:
In this tutorial, we will proceed to give an overview of the exciting field of AI and HPC. It will cover the critical and special characteristics and the architecture of the popular AI chips. Next we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips. We will also look at how the shift to 2.5D and 3D including Chiplet development is changing the industry and the adding new challenges for the DFT community Finally, we will present a few case studies on how DFT is implemented in the real AI chips. We will also present some of the functional monitoring techniques that are available today. An overall architecture showing how functional monitoring can be implemented and how the monitor data can be used to manage in-life capabilities. Finally, we will present a few case studies on how DFT is implemented in the real AI chips.

Lee Harrison is Product Marketing Director, with the Tessent product division at Siemens EDA. He has over 20 years of industry experience with Mentor DFT products and has been involved in the specification of new test features and methodologies for Mentor customers, delivering high quality DFT solutions. With a focus on Automotive, Lee is working to ensure that current and future DFT requirements of Mentor's Automotive customers are understood and met. Lee Received his BEng in MicroElectronic Engineering from Brunel University London in 1996. Lee presents regularly at industry conferences such as DAC, ITC, VTS, ETS, DATE etc.

Peter Orlando is the SSN Product manager and part of the Siemens Tessent DFT Product Marketing team. Since joining Siemens 2018, Peter has been part of the development of SSN product and primarily responsible of the deployment of SSN. As the customer facing technical lead for the SSN product, Pete has been providing implementation guidance to external customers and internal colleagues. He's been part of many designs that have successfully taped out with SSN. Pete's role in SSN continues to expand with the development and deployment of new features being added to regularly.

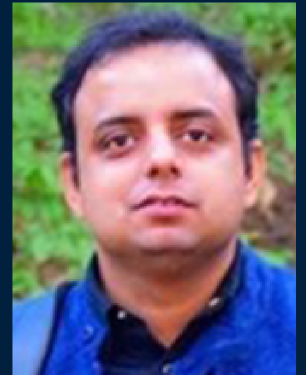
Tutorial 8

Hardware Security: A perspective towards Fault Analysis Vulnerabilities

Sunday July 23, 2023

Tutorial Summary:
In this tutorial, we focus on hardware security aspects that exist in the present-day IC industry. The tutorial will mainly focus on different types of fault analysis attacks that bother ICs and their security applications when deployed in field. Over the past decade, IoT devices are becoming more ubiquitous, and are often exposed to attacks that are device specific. One such class of attacks is fault attack. With unprecedented level of embedded technology and device connectivity, security an privacy of user data has emerged as paramount importance. In general, secure computations through the use of cryptographic modules has been the primary mechanisms to alleviate such concern. However, crypto-processors that implement such modules have themselves been subjected to implementation attacks, such as sidechannel and fault injection analysis. Given the fact that a large number of embedded devices are significantly resource-constrained with low processing power and memory availability, provably-secure and mathematically robust lightweight cryptographic architectures and constraints do exist in literature. However, security in theory is more often different from practice, with many a sip between the cup and the lip. One such sip that we will focus on are implementation-based attacks on embedded devices with the ability to weaken even cryptographic primitives that cater to world-wide standard specifications.

Dr. Bodhisatwa Mazumdar is an Associate Professor in the Department of Computer Science and Engineering, and Associate Dean-R&D II, at IIT Indore. He earned his M.S. and Ph.D. degrees from the Indian Institute of Technology (IIT) Kharagpur, Kharagpur, India. He was a Postdoctoral Researcher with the Design for Excellence Laboratory, New York University Abu Dhabi, Abu Dhabi, UAE. His current research interests include optimized hardware implementations of cryptographic primitives, and side channel attacks and countermeasures.



He is presently a voting-cum working group member (WGM) in IEEE Standard 1413.1 on Guide for Selecting and Using Reliability Predictions, and IEEE 1624, which is the IEEE Standard for Organizational and Capability. He has received Early Career Research Award from CSIR, New Delhi. Dr. Mazumdar has been a Technical Program Committee Member of conferences, such as VLSID, SPACE, and VDAT, and is one of the Program Chairs of SPACE 2023 conferences.

Tutorial 9

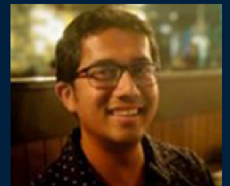
Power Aware DFT

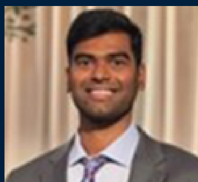
Sunday July 23, 2023

Tutorial Summary:

Power Handling during Test is an important factor that needs to be considered during chip design, silicon bring-up, and In-System Testing. In this tutorial, we will start by listing the importance of power and the different problems faced with poor power intent. We will then proceed to give an overview of different power aspects related to test, from RTL implementation to in-system validation, and how each step can impact the overall performance. Next, we will introduce the different DFT techniques for design that help with better power planning producing optimized quality of results (QoR). Finally, we will present data sets on how each of the listed techniques implemented on real designs give the desired results. This tutorial will include the following three parts (each part will be 20 minutes): Memory and Scan Test Implementation, Scan Synthesis, Placement and Routing, Automatic Pattern Generation.

Karthik Natarajan is a Director in Synopsys Test group. He has more than 14 years of experience in Design for Test from Architecting DFT for complex SoC's to Silicon Bringup & Yield Ramp. He has multiple patents and papers in the field of Test.





Likith Manchukonda is a Sr. Solutions Engineer in Synopsys Test group. He has more than 7 years of combined experience in CAD, circuit design and in DFT from test architecting to silicon bringup.

Manish Arora is a Sr. Solutions Manager in Synopsys Test group. He has 16 years of experience in DFT with prominent companies like Freescale and AMD. He has a broad experience in memory test and repair for various end applications like automotive, mobile and CPU/GPU designs.

Rahul Singhal is a Product Manager for TestMAX DFT, ATPG and Test-AI products at Synopsys. His focus is on the industry requirements and solutions in the areas of test compression, test streaming solutions and ATPG. He has co-authored multiple tutorials, papers, posters on test in leading IEEE conferences. Rahul received his MS in Electrical Engineering from Portland State University and BS in Electrical Engineering from Purdue University.

Greeshma Jayakumar is a Staff Application Engineer in Synopsys Test Group where she is leading the India regional customer support on the Synopsys TestMAX family of products. She has overall 11 years of experience in the DFT industry and has worked on test architecture, methodology, ATPG & Silicon bring up.

Keynote 1

Can Structural Test play a role in mitigating Silent Data Errors?

Monday July 24, 2023, 9:30 - 10:15am

Abstract:
The evolution and continuous growth of data-intensive applications such as AI/ML, IoT, blockchain, etc. have fueled the rise of hyperscale datacenters across the world (including India). It is forecasted that the number of such hyperscale datacenters will exceed one thousand by 2026 (Synergy Research Group). One of the biggest challenges facing such hyperscale datacenters is Silent Data Error (a.k.a. Silent Data Corruption). Silent Data Error (SDE) is an industry-wide phenomenon that not only impacts memories, storage, and networking but also CPUs. Technology scaling, system scaling, increased density, and wide data-paths have been identified as key contributors to such errors. SDE tends to be very elusive as it is not traceable at the hardware level but manifests as an application-level problem with potentially devastating impact on datacenter reliability and availability. More importantly, such failures occur at specific environmental conditions (power, temperature, and voltage profiles) in a system running applications creating targeted software workloads. In recent years, there has been a lot of discussion emphasizing the role of manufacturing test escapes on SDE. Additional factors such as design marginalities, latent/intermittent defects, and transistor aging potentially also impact the behavior of silicon in-field. In this talk, we will explore how structural test can play an important role in alleviating Silent Data Error. We will not only look at ways to improve test quality, but also highlight a hierarchical, scalable, and adaptive DFT infrastructure, needed for various phases of test including continuous monitoring of electronic devices throughout the silicon lifecycle.

Nilanjan Mukherjee is a Senior Director of Engineering for Tessent Silicon Lifecyle Solutions at Siemens EDA. He has been actively involved in the R&D of key technologies in the areas of test quality, test compression, Logic BIST, Memory BIST, low power DFT, and diagnosis. Specifically, he was involved in the development and productization of EDT/TestKompress, the VersaPoint Test Points technology, a Low Power Hybrid EDT/Logic BIST scheme for automotive ICs, and Observation Scan Technology for Logic BIST. More recently his focus is on developing new in-system/in-field test solutions based on deterministic patterns (In-system TestKompress) including silicon lifecycle management for automotive and data-center markets.

Keynote 2

Test industry challenges and solutions as observed by the leading physical implementation solution provider

Monday July 24, 2023, 10:15 - 11:00am

Abstract:

Test is a mission critical aspect of the design process, but design functionality/verification consumes the significant majority of engineering focus, with test often retrofitted late in the design cycle. The era of point-tools is over, what's needed is deep collaboration across the flow from state-of-the-art design IP, verification, physical design, and packaging. New solutions must manage test structures from multiple sources and meet coverage, test time, and PPA goals without introducing design closure iterations. This presentation offers a new way forward, borne from Cadence's unique perspective gained from experience working with global semiconductor suppliers engineering test into some of the world's most complicated designs.

Janet Olson is Vice President Research and Development for Front-End Design at Cadence Design Systems. Janet is responsible for Modus, Cadence's IC test solution, high level synthesis (Stratus) and constraint verification (Litmus). Janet has a master's degree in Electrical Engineering from Stanford and a bachelor's degree from CMU and holds 7 US patents. Janet has been recognized with the 2017 Marie R. Pistilli Electronic Design Award and the 2016 YWCA Tribute to Women award.

Keynote 3

Disruptive Technologies Drive a New Era of Test

Tuesday July 25, 2023, 09:30 - 10:15am

Abstract:

The semiconductor test community is facing multiple challenges driven by the ever-growing performance and reliability expectations of today's cutting-edge technology. Modern designs have increased test coverage, quality and accuracy requirements and mounting test costs mean even more pressure to reduce time on the tester. Leveraging disruptive technologies, such as unlimited compute and AI capabilities is the key to providing solutions to these challenges, unlocking a whole new era of test capabilities and efficiencies. This keynote will explore two fundamental areas where disruptive technologies are already starting to have a positive impact on semiconductor test. Firstly, Time to Results (TTR) is a critical factor when it comes to successfully scaling the design cycle and these latest developments are allowing test engineers to implement test time reductions while maintaining high levels of quality and performance. Secondly, advances in AI have enabled much higher quality test pattern generation and this is already proving beneficial as part of a solution to address new industry challenges such as Silent Data Corruption (SDC), where undetected hardware logic failures can result in incorrect data results. These advancements in combination with the emerging paradigm of Silicon Lifecycle Management (SLM) are signaling a new era of Semiconductor Test.

Fadi Maamari is Vice President of Engineering in the Hardware Analytics and Test group of Synopsys, responsible for the TestMAX Product line. He joined Synopsys in the 2015 acquisition of Atrenta, where he was Chief Product Architect. He was previously Vice President of Engineering and COO of LogicVision when it was acquired by Mentor in 2009. Fadi has a Ph.D. in Electrical Engineering from McGill University in Montreal, and started his career at AT&T Bell Labs working on various EDA algorithms and Design For Test.

Keynote 4

Paradigm Shift: Structural Approaches to Analog and RF Test

Tuesday July 25, 2023, 10:15 - 11:00am

Abstract:

Analog and RF test has been considered to be a niche domain where test patterns are developed based on experience of the test engineer and specifications of the product. This approach worked well particularly when analog and RF circuits have been implemented by mature processes where defect rates were better controlled. Even then, this ad-hoc testing process leaves the IC vendors with no quantitative metric of defect defect coverage and no recourse if testability becomes a major bottleneck for time-to-market. Seemingly endless integration of system components, including RF devices on a single die or package requires a paradigm shift for testing analog and RF devices. Structural approaches to testing, built-in test, and test quality metrics are needed. This presentation provides a historical context for structural test efforts as well as provide a sneak peek into the future of structural testing and test quality metrics in the analog domain.

Sule Ozev obtained her B.S. degree in Electrical Engineering from Bogazici University, Turkey in 1995, and her Ph.D. in Computer Science and Engineering from UC San Diego, USA in 2002. She has been a faculty member, first at Duke University and then at Arizona State University since 2002. Her research interests include test methods, statistical test metrics, and built-in test for analog/RF circuits as well as MEMS devices. She has published over 200 papers in this domain and has won 8 best paper and honourable mention awards at various IEEE conferences. She holds 4 US patents.

Panel Discussion

Voltage bump decisions to work around Vmin issues for structural tests: are these based on any science or pure tribal art?

Panelists:

- **Jais Abraham (Qualcomm)**
- **Srinivas Vooka (Google)**
- **Prasad Mantri (AISemiCon)**
- **Steve Palosh (Cadence)**
- **Malav Shah (Texas Instruments)**

Moderator: Kamlesh Pandey (Qualcomm)

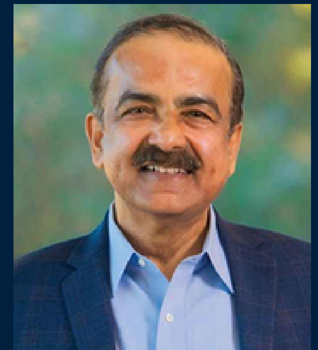
Abstract: Modern day SOCs are aggressively designed to consume the lowest possible power to achieve desired performance. The SOCs operate in multiple operating modes defined by voltage and frequency combinations. To guarantee robust operation, the SOCs are tested in each operating mode by applying structural and functional tests. The structural tests, comprising of memory BIST and variety of ATPG patterns, often encounter minimum operating voltage (Vmin) margin problems during phasing/volume testing. To recover yield, problematic patterns are replaced with low switching versions. Generally low toggle patterns generation step is iterated several times before the stable pattern set can be found. Beyond low toggle patterns and occasionally masking some scan cells based on failure diagnosis, some voltage bump is applied to make certain structural tests robust and eliminate yield loss. In this panel discussion, we will focus on various criteria applied in industry to determine acceptable voltage bump to address Vmin issues during post silicon debug phase. The panel will ponder upon the following questions/topics.

1. What are possible physical defect mechanisms that can cause Vmin marginality issues?
2. What are the reasons behind Vmin issues seen predominantly in structural tests whereas functional tests rarely require voltage bump?
3. How to find out if further reduction of switching activities will not improve Vmin margin?
4. What are the possibilities and nature of some real defects escaping due to voltage bump application?
5. Will voltage bump result into any reliability issues in future?
6. Is it possible to predict Vmin marginality and take preventive actions during PDN design?
7. Can Vmin issues be eliminated by carefully adding some additional margins in STA signoff recipe?
8. Why does each design module have different Vmin margin despite using same timing closure and physical implementation recipes across entire SOC?
9. Are there any significant differences between logic Vmin and memory Vmin marginalities?

Invited Talk 1

Circuit Timing Marginalities and Silent Data Corruption

Abstract: Recent presentations from Google and Facebook (Meta) have reported significant levels of silent data corruption in their large data centers. These transient errors, which can go undetected for long periods and are extremely difficult to diagnose and root cause, have been correlated with specific processor cores in large processor networks, suggesting faulty or unstable hardware. We suggest that a possible cause of these failures are statistically rare outlier circuit paths displaying marginal timing due to unavoidable random variations in the manufacturing processes. Since switching delays are dependent on circuit state and environmental conditions, some marginal paths can escape detection during postproduction testing, but still cause occasional failure under worse case conditions in operation. We present analysis from research that is studying the impact of random process variations on the timing of CMOS gates and circuit paths when operating at significantly reduced voltages. Circuit delays are accentuated in low voltage, power saving operational modes commonly employed by thermal management in advanced processors, increasing the likelihood of timing failures.



Adit Singh is Godbold Endowed Chair and Professor of Electrical and Computer Engineering at Auburn University, USA. He earlier served on the faculties of the University of Massachusetts in Amherst, and Virginia Tech in Blacksburg, and has held visiting positions at the University of Tokyo, Japan, the Universities of Freiburg and Potsdam in Germany, the Indian Institutes of Technology, and as a Fulbright scholar at the University Polytechnic of Catalonia in Barcelona, Spain.

EHis technical interests span all aspects of VLSI technology, in particular integrated circuit test and reliability. He has published over three hundred research papers and holds international patents that have been licensed to industry. He has served as a consultant to several semiconductor and EDA companies, including as an expert witness for major patent litigation cases. He has had leadership roles as General Chair/Co-Chair/Program Chair for dozens of international VLSI design and test conferences. He served two terms (2007-11) as Chair of the IEEE Test Technology Technical Council (TTTC), and (2011-15) on the Board of Governors of the IEEE Council on Design Automation (CEDA). Singh received his B.Tech from IIT Kanpur, and the M.S. and Ph.D. from Virginia Tech, all in Electrical Engineering. He is a Life Fellow of IEEE.

Invited Talk 2

Methodologies to evaluate Robustness of Modern Complex SoCs

Abstract:

Modern electronic systems use semiconductor components within tight specifications/limits. It is very important to understand how these semiconductor components actually perform within and outside these specification limits. This understanding can help in overall system optimization towards better Power, Performance, and cost. Alternatively this knowledge can be used to provide an additional guard band for semiconductor component's functionality. Therefore, understanding Robustness of semiconductors help in achieving lower ppm-failure rates by ensuring sufficient guard band between the operating range of the semiconductor and the points at which the semiconductor fails. Robustness Validation (RV) is a process to check functionality of a semiconductor IC for a given application profile. RV utilizes the understanding of the IC (analog, digital, other) failure mechanisms thereby providing key feedback to improve the IC within and outside the datasheet limits. Understanding the timing, power delivery network and physical implementation aspects of modern SoCs (System-on-Chips) can help in improving Robustness margin for a key semiconductors components (such as Microprocessors, Microcontrollers, ASICs, etc). This RV methodology can be applied to all electronic components within a system, thereby significantly increasing the overall system robustness.

Surya Musunuri is Silicon Architect working on Aurix microcontrollers at Infineon Technologies. Before Infineon, Surya worked for Apple Inc, Cupertino, USA, where he was responsible for Hardware Power Management features of iPhone. Prior to Apple, he worked at Intel Corporation on developing IPs such as Voltage Regulators, PLLs, Clock Control Units, Random Number Generators and Security Units. Over the years at both Intel and Apple, he worked on several topics related Clock, Power, High-speed IOs for PC, Server, ultramobile and Smartphone platforms.

Surya graduated with Masters and PhD degrees in Electrical and Computer Engineering from University of Illinois at Urbana Champaign, where his research focused on integrated voltage regulators. He also has a Masters Certificate on Systems Design from Massachusetts Institute of Technology. Outside work, Surya's interests include Biking, Hiking, Table Tennis and Tennis.

Technical Session 1

MBIST Test Challenges | Session Chair: Sandeep Jain

1.1 Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation

Nikhil Karkare and Wilson Pradeep

Power, performance and area (PPA) are the three key differentiating factors in today's SoCs (System on-chips). To achieve best-in class PPA, complex processor cores using shared bus architecture typically use single physical memory across multiple logical memories to improve overall design efficiency. However, such an implementation imposes several limitations on enabling redundancy and repair support using on-chip memory test, redundancy analysis and repair implementation for the full range of memory space, resulting in a degraded repair coverage. This in turn could result in inferior yield and thereby increase cost margin for the product. In this paper, we propose a few novel strategies to seamlessly enable redundancy sharing across logical memories shared by a single physical memory to mitigate the limitation with conventional approaches. Additional schemes are proposed to resolve potential conflict conditions that could arise as a result of this redundancy sharing. Furthermore a comprehensive fault injection and repair verification methodology is shared to assess the efficacy of proposed methods. The experimental results by using the proposed solutions on two sample clusters on a large-scale design using shared bus architecture bridged a gap of 5-6% drop in repair coverage due to the shared physical memory implementation.

1.2 MBIST-HSIO Concurrent Testing Strategies and Test Challenges

Boopala Krishnan, Shalini Mishra, Sumit Emekar, Subrahmanya M, Prasanna Ramanujam, Melvin Cu and Linfeng Pu

Semiconductor chips are getting complicated with increasing transistor density onto the same mm2 area. As the complexity of chips increases, test cost surges since it holds a significantly larger part on the Silicon design process. Test-Time is one of the key parameters which decides per chip test cost. The methodology proposed in this paper helps to reduce the test cost significantly. This paper focusses on the strategies defined by the authors to enable concurrent testing between two major testing blocks HSIO and MBIST. Both the blocks have a lot of variation on vector structure and way in which they are tested. The paper discusses the challenges that authors have faced during implementation and silicon bring-up. Finally, the paper highlights the savings that's been seen across designs where this approach has been implemented.

Technical Session 1

MBIST Test Challenges | Session Chair: Sandeep Jain

1.3 MBIST Area & Test Time Optimization Using Machine Learning Techniques
Darakshan Jamal and Ratheesh Thekke Veetil

In System-on-Chip (SoC) designs, a significant portion of the die area is allocated to Design for Test (DFT) logic, with a substantial fraction dedicated to Memory Builtin Self-Test (MBIST) functions. This results in significant perpart test costs, impacting the overall chip cost. To increase profit margins and achieve cost savings, it is crucial to optimize the MBIST area while balancing test time and considering physical design challenges. The exploration of different memory groupings, MBIST strategy and their associated physical design challenges can be a time-consuming task. Due to resource and schedule constraints, conducting multiple iterations during the project execution to arrive at optimal MBIST design becomes impractical. In this paper, we propose the use of machine learning (ML) algorithms to address the optimization of memory grouping and MBIST strategies. By leveraging ML models, we aim to identify the most suitable memory grouping and MBIST strategy that results in an optimized MBIST design. We can achieve better physical design metrics by applying the proposed ML model to generate RTL, including improved timing, reduced congestion, and a smaller area footprint. Overall, our research demonstrates the potential of ML algorithms in optimizing the MBIST area and test time, leading to significant cost savings and improved profit margins in SoC designs.

Technical Session 2

Productivity Enhancement through Improved Diagnosis | Session Chair: Veejaye Panayadian

2.1 A novel test data compaction method with improved debug capabilities of the signatures
Jaidev Shenoy, Kelly Ockunzzi and Dr. Virendra Singh

Built-In Self Test (BIST) is mandatory in current day automotive ICs and widely adopts space and time compaction methods like Multiple Input Signature Registers (MISRs). The BIST methods are primarily used during in-field testing to identify only pass/fail without much focus on debug/diagnostics due to compaction of large number of bits. In this paper, we have introduced a novel space and time compaction scheme which identifies the exact location of fault capturing scan cells using simple signature analysis based on elementary mathematics, improving the debug capabilities. Along with the mathematical proofs, we also demonstrate the added advantages of this scheme in terms of scalability, ability to adopt existing top-off on-chip signature comparison methods which makes it flexible to be used in both manufacturing and in-field testing. The validation process of the proposed idea have also been discussed , including the results wherein for every simulation, we obtain 100% accuracy. The hardware implementation options have also been discussed briefly.

Technical Session 2

Productivity Enhancement through Improved Diagnosis | Session Chair: Veejaye Panayadian

2.2 A novel approach to identifying scan issues during RTL validation

Alli Sravan, Malagiri Shashi Vardhan Reddy, Velamala Nithin and Ravathkar Ashwin Kumar

As we know, today's system-on-chip designs are complex with billions of transistors on it making it very difficult to test. A module may behave properly in terms of its functionality during the designing of the chip, but it also should be ensured that every module in SOC must function properly in post-silicon. As the process of manufacturing requires fine precision, the chip must undergo testing during its designing phase. As a part of testing in SoC, it's of utmost importance to insert DFT (Design for Testing) components into all the IPs and the modules present in the SOC. Each soc can have hundreds of partitions and contain thousands of flops. During scan insertion, these flops are converted into scan flops to perform scan-based testing to increase the controllability and observability on the internal nodes of the circuit. During the conversion of flops into scan flops by ATPG, some of the non-scan flops which are part of critical signals such as Power switches, PLLs, Resets, etc., may also get converted and become part of the scan. In ATPG, validation happens at the partition level and these critical signals are provided with cut points. So, any toggle in the power switches will not affect the ATPG simulations. In soc, any glitch at the input of the clocks may cause the flops to capture an unsolicited value which may corrupt the power domain and PLLs may also lose their lock. These types of issues can be caught in full-level GLS where the design is very large and debugging these errors is a humongous task that is also at the very end of the cycle. In this paper, we discuss how to catch the issues mentioned above, early in the RTL cycle itself rather than going to the end of the cycle. By catching these issues, we reduce test cycle time, improve the quality of the chip, and hence reduce the cost of the chip.

2.3 Addressing physically aware diagnosis challenges in hierarchical core based designs

Bharath Nandakumar, Sameer Chillarige, Robert C Redburn, Jeff Zimmerman and Nicholai L'Esperance

Hierarchical Test (HT) is a partitioned-test method designed to improve performance and decrease resources costs in both DFT and test. Specifically, this methodology eases computing resources and run times required for automatic test pattern generation. It also presents unique challenges and opportunities for diagnosis. Physically aware volume diagnostics greatly improves callout resolution, enabling diagnosis of new fault types, but presents scalability and deployability issues for hierarchical core-based designs. This paper highlights solutions needed to create an efficient high-volume physical diagnosis pipeline for hierarchical core-based designs. Results of the proposed system are demonstrated on 7nm processor designs.

Technical Session 3

AI/ML in Test | Session Chair: Jyotirmoy Saikia

3.1 Application of Machine Learning in De-embedding of Signal Integrity Parameters for High Speed Serial Link

Maneesh Pandey, Mohit Goyal and Ajay Dash

This Signal Integrity measurements are imperative to High-Speed Serial Link characterization. However, as new protocol definitions introduce higher data rates and enhanced tighter specifications, the characterization activity becomes challenging with existing equipment. The labs need to update the hardware measurement equipment and/or update the measurement software in the existing equipment. For multiple characterization setups, as in a typical industry lab activity, this adds to the significant monetary cost to support newer protocols. Moreover, some measurements like signal de-embedding need multiple measurements based on protocols being tested. This leads to time overhead in overall validation activity. Thus, there is a need to develop techniques that can reduce the expenditure and save test time with minimal impact on the measurement accuracy.

3.2 Machine Learning Based MBIST Area Estimation

Puneet Arora, Virad Jain, Tarun Goyal and Norman Card

Majority of the silicon with-in a design is occupied by memories. Memories are more prone to failures than logic due to their density. Several techniques have been established to target and detect defects within these memory instances and their interfacing logic. The most widely used approach is memory built-in self-test (MBIST) that inserts on-chip hardware unit(s) which provides systematic method of writing and reading data patterns to and from the memories. The MBIST hardware also performs the failure analysis and, when redundant resources exist, repair these memories. The number of MBIST units and heir area depend upon the configuration that designers chose for memory testing based on test requirements like power, test-time, repair, programmability, algorithms and so on. With more and more functionalities being present on chip, silicon real estate is becoming crucial than ever. This puts a lot of pressure on the amount of area that can be used by MBIST unit(s). This makes it very important to estimate the area with very high accuracy to decide the configuration for memory testing. This paper describes a machine learning (ML) based approach to estimate the MBIST logic area in seconds for different configurations without synthesizing the design to avoid costly design cycle iterations with an accuracy of more than 90% and help designers to choose the best possible configuration for memory testing.

Technical Session 3

AI/ML in Test | Session Chair: Jyotirmoy Saikia

3.3 Hardware Simulator : Virtual Testing and Non-Product Failure Isolation

Akhila K, Shalini Srinivasan N, Gopikrishnan K and Harish G L

This paper introduces a novel approach to detect and isolate failures in manufacturing production lines through a hardware simulator without actual hardware. It employs multiple emulation techniques to accurately replicate different system scenarios, which also helps in rapid isolation of faults & non-product failures, recovery, debugging & reporting for actions.

Technical Session 4

Power Aware DFT & Functional Test | Session Chair: Raghu GG

4.1 Power Domain Aware DFT Implementation

Sarthak Singhal, Subhasish Mukherjee, Christos Papameletis, Krishna Chakravadhanula, Ankit Bandejia, Dale Meehl, Archana Vyas and Mohan Gandla

Power awareness has become an important dimension for recent advances in VLSI. Multiple functional power domains (PD) are forcing Design-for-Test (DFT) designers to adjust DFT insertion and implementation to comply with IEEE 1801 correctness. Several challenges emerge for DFT tools and engineers, including but not restricted to a) additional low power cells inserted & crossings created due to DFT connections, b) power aware scan chain connection with optimal scan wirelength, and c) ensuring Unified Power Format (UPF) correctness post DFT insertion. This paper describes power domain aware DFT techniques for core wrapping, heterogenous fanouts and PD fencing aware scan chain stitching. A correct by construction approach results in fewer low power cells, improved scan wirelength & fewer IEEE 1801 rule violations. The EDA automation demonstrated in this paper reduces the manual overhead for chip designers to ensure power correctness of the design after DFT implementation.

Technical Session 4

Power Aware DFT & Functional Test | Session Chair: Raghu GG

4.2 Design of a Fault-Tolerant Pseudo-3D Routing

Biswajit R Bhowmik and Gagan N

Networks-on-chip (NoCs) are often exposed to faults that disturb the overall network performance. Subsequently, fault-tolerant routing algorithms have become one of the most holistic aspects of reliable NoC communications. This paper proposes a pseudo-3D mesh architecture-specific fault-tolerant routing algorithm. The concept of a detour path is the foundation of the proposed solution. Its goal is to ensure the delivery of almost all packets with a detour of a few without utilizing broken or faulty communication functionalities. On evaluations, the suggested technique produces 11.47% greater throughput, 38.38% lesser latency and 65.50% improved energy consumption compared to the baseline mesh NoC. Based on the findings, one may conclude that the proposed fault-tolerant routing performs more effectively even at higher traffic load levels.

4.3 Parallel Functional Test : A case study to reduce test cost in large SOCs

Akshatha P Inamdar, Syed Shadab and Karthik Chandrashekar

In modern SOCs, test cost reduction has become a key goal. Test cost contributes to a good part of the die cost and all efforts to minimize the cost are critical to enable good product profit margins and eventually lead to the success of a product. The time taken by each functional test for each IP in the die will contribute to the overall test cost of the SOC. The SOCs contain many design modules integrated into them and testing each of these modules one by one is a tedious and timeconsuming process. When we are testing an IP or a group of IPs in the SOC, the rest of the IPs in the chip are in an idle state. Testing all the IPs takes a very long time to cover a single chip, especially on large SOCs. In this paper, we propose a generic solution to reduce the overall test time and hence the test cost. The testing of modules is performed in a simultaneous manner so that at a given time, several IPs can be tested in parallel. We put forth two scenarios of test time optimization. First one being running Memory built-in self-test and Physical layer test in parallel. Second scenario is testing the PLLs across different IPs in a die at the same time. On doing so, in first scenario, we reduce the test time of a die by about 32.43% and about 56.2% using the second one. When this is applied on a large scale on multiple dies, we will be saving a significant amount of time and therefore, improving the cost of testing and profit margins of the product.

Technical Session 5

Advances in security | Session Chair | Prof. Priyank Kalla

5.1 Invisible Scan for Protecting against Scan-based Attacks: You Can't Attack What You Can't See

Pravin Gaikwad, Patanjali Slpsk and Swarup Bhunia

Scan-based Design-for-Test (DfT) infrastructure renders an ASIC design testable by making internal circuit nodes more controllable and observable. It, however, vastly conflicts with the security requirements of a design by making on-chip assets vulnerable to scan-based attacks. To address this critical security issue, over the past two decades, numerous scan protection solutions have been investigated. However, none of the existing solutions addresses the growing need to protect a scan chain under the emergent zero trust model. This model considers a fully untrusted fabrication and testing facility consistent with the modern globally distributed supply chain ecosystem. Under this model, existing protection against scan-based DfT can be easily bypassed, leading to unauthorized scan access. This work, for the first time, analyzes the vulnerabilities of state-of-the-art scan countermeasures and presents InvisibleScan, an innovative state space obfuscation-based scan protection method to prevent scan attacks under zero trust. We evaluate InvisbleScan on a suite of ITC'99 benchmarks and show that it incurs minimal overhead while providing strong security guarantees.

5.2 Hidden in Plain Sight: A Detailed Investigation of Selectively Increasing Local Density to Camouflage and Robustify Against Optical Probing Attacks

Sajjad Parvin, Chandan Kumar Jha, Sallar Ahmadi-Pour, Frank Sill Torres and Rolf Drechsler

Modern chips have been demonstrated to be vulnerable to malicious Side-Channel Analysis (SCA) attacks that put Intellectual Property (IP) at risk. These SCA attacks and their countermeasures have been well-studied in literature. However, in recent years a non-invasive and laser-based SCA attack through the backside of chips, namely Optical Probing Attack (OPA), has emerged. OPA is effective in retrieving the chip's IP by reading out the transistors' terminal voltage. Some countermeasures to mitigate OPA have been proposed in the literature. However, these methods are too expensive to implement as they require significant change in the fabrication process. These existing methods require a whole redesign of logic cells layout, characterization, synthesis, and place and route techniques which can be quite challenging.
In this work, we investigate the effect of increasing the density around an important logic cell in the design, that needs to be secured against OPA. Our methodology requires only the standard cell library gates and can be easily integrated into the ASIC design flow. We found that increasing the local density of cells around an important logic cell can lead to a larger reflection. This can significantly help to camouflage the secure cell against OPA, as the reflection from the secure cell and the neighboring cells can be hard to differentiate. We show that this methodology can prove to be an effective countermeasure against OPA by performing detailed experiments of density versus reflection using nand and inverter cells. We exhaustively [illegible]ed thousands of placement strategies with varying densities to show its efficacy against OPA.

Technical Session 5

Advances in security | Session Chair | Prof. Priyank Kalla

5.3 PROTECTS: Secure Provisioning of System-on-Chip Assets in Untrusted Testing Facility
Patanjali Slpsk, Jonathan Cruz, Sandip Ray and Swarup Bhunia

System-on-Chips contain variety of Hardware Security Assets (HSAs) to protect the components of the system against untrusted entities. Binding the HSAs to each SoC silicon instance during the testing stage, known as provisioning, is a critical step in SoC life cycle since improper provisioning could compromise the secure, trustworthy field operation of SoC and/or lead to crucial supply chain threats (e.g., piracy, cloning and reverse engineering). However, existing SoC provisioning methods do not scale to more advanced threat vectors under the emergent zero trust model that considers the foundry and testing/assembly process untrustworthy. We address this problem through a comprehensive framework, PROTECTS that enables secure provisioning of HSAs under zero trust. We demonstrate PROTECTS using a representative RISC-V based SoC with diverse set of HSAs. Our analysis shows that PROTECTS incurs minimal design overheads (0.36%, 0.54% and 0.0%) in area, power, and gate-count, respectively, for the entire SoC), while providing strong security guarantees.

Technical Session 6

Validation & Test Methodologies | Session Chair: Balaji Upputuri

6.1 Scalable and Comprehensive approach for Concurrency Validation to improve Platform Stability
Naveena Nataraj, Jayaprakash Bs, Chockalingam A, Mandira Kumar Sathanantham, Kishore Chittudi, Ravishankar S, Abhishek Paliwal and Nihar Ranjan Saha

Recent decades have seen an increase in integration of multiple components and cores in client platforms. Computing systems are evolving to meet ever-growing needs to provide concurrent performance across CPU, Graphics and other platform domains. This paper describes a methodical approach to Generate, Execute and Verify Concurrent Use-cases and Analytics solutions.

Technical Session 6

Validation & Test Methodologies | Session Chair: Balaji Upputuri

6.2 A formal approach to improve connectivity coverage in DFD, DFT, DFM, and DFX domain
Jayashri Patil, Kruttika Golwelker, Manu Yeeshu, Sood Surinder, Ananth Deepak K. S. and Shruti Deshpande

The aim of this paper is to analyze the coverage with formal verification for the debug fabric in the SOC in such a way that it will left-shift the validation process to enhance validation productivity beyond its primary goal of finding bugs at an early stage. By using the formal coverage matrix designers identify areas of the system that require additional verification and ensure that the system meets the highest standards of quality and efficiency. A case study of formal verification of a complex debug network of observe-pin mux spread across the complete SOC is explained in this paper.

6.3 Prevention of High Current Events during Hot Testing at Turbo Frequency
Navaneeth A, Tiwari Himanshu, Sankapal Dudapa B and Vetcha Anand S

This paper discusses about new approaches to resolve the high current events that could occur on the ATE. The high current events can occur at hot temperature when the testing is done at turbo frequency. Multiple occurrences of these events can lead to the chip getting burned and unrecoverable.

Technical Session 7

Overcoming Analog/Mixed-Signal Test Challenges | Session Chair: Prof. Sivanantham

7.1 Analysis of Non-idealities in On-chip Loopback Testing of Data Converters
Tamajeet Mandal, Aswin R and Rubin Parekhji

The demanding linearity requirement of an on-chip ramp generator for ADC built-in self-test (BIST) has paved the way for alternative testing routes. Loopback testing has emerged as a substitute, in which another component, for example a DAC, in the same chip is used as the ramp stimulus, significantly reducing the cost incurred due to the need for an automatic test equipment (ATE). However, fault cancellations in loopback tests can lead to faulty units being undetected in production and thereby test escapes. This work analyzes non-idealities leading to test escapes in case of an ADC to DAC loopback test. Experiments have been performed on 2 types of DAC and one type of ADC using MATLAB models. Results indicate that, with specific fault injections, out of a total of ten different DAC to ADC loopback configurations, six resulted in fault detection while four resulted n faults getting masked. A few test and design methods are also proposed to mitigate such fault masking.

Technical Session 7

Overcoming Analog/Mixed-Signal Test Challenges | Session Chair: Prof. S. Sivanantham

7.2 Unified Analog Mixed-Signal Defect Simulation and Applications

Krishna Kumar Ganapathy Raman, Aswin R, Arshad Qureshi, Supraja R, Chanakya K V, Vijay Kumar Sankaran, Vinay Rawat, Victor Zhuk and Lakshmanan Balasubramanian

Ensuring test program readiness, efficiency of post-fabrication debug/diagnostics, test cost and quality entitlement are critical vectors contributing to the success of analog and mixed-signal (AMS) ICs. In this paper we will discuss some of the impactful recent developments in analog defect/fault simulation (AFS) that is at the center of all of these vectors. The features that we will discuss include the following: a) Unified analog and digital fault simulation framework to enable holistic and efficient analysis of AMS designs; b) Utilising physical design i.e., layout information to improve practicality and efficiency of AFS campaign. The need, application challenges, solutions to overcome them and possible future directions will be highlighted through appropriate industrial case studies.

7.3 An SoC based Cost Effective Static Linearity Test Scheme for ADCs

P R R K Tirumalesu Manda and Keerthan Rai

This paper discusses a cost-effective static linearity test method for SoC based ADCs. It reduces the cost of data acquisition and improves quality of test. For a 12-bit, 1 Msps ADC, post-processing time reduces by 80% and memory required to post-process linearity reduces from 4.5 MB to 16 KB or 8 KB.

ART

Session Chair: Prof. Usha Mehta & Sandeep Jain

ART 1.1. Quality metric based optimal test option generation for small delay defects

M Prathiba and S Sivanantham

ART 1.2. Lightweight Secured Split Test Technique with RMA Capability for Integrated Circuits

Sudeendra Kumar K, Akshay Girish Kaushik, Adithya B Shetty, Ashutosh Rao and Akshay S

ART 1.3. Detection of hardware Trojans using Decision Tree Classifier at RTL of an ICs present in IoTs

Lavanya T and Dr Rajalakshmi K

Test Reality Check

Session Chair: Vishal Vadhavania & Dimple Aggarwal

TRC 1.1 HTOL Vector Utility(VecUtil) Tool For Protocol Aware Vectors

Boopala Krishnan, Shalini Mishra, Prasanna Ramanujam and Subrahmanya M

TRC 1.2 Curious Case of Fab Process Variation on PLL Lock

Ajmal Firdous, Syed Feruz Syed Farooq, Himanshu Tiwari, Govil Badghare, Rucha Rathi and Kishore Kumar Banda

TRC 1.3 Design/Manufacturing Challenges & Solution for highly Dense and large ATE DUT Boards

Rajiv Vk

TRC 1.4 Novel Methodology to Optimize TAT and Resource utilization for ATPG Simulations for Large SoCs

Sudhakar Kongala, Anuj Gupta, Yash Walia and Sahil Jain

Posters

Session Chair: Bharath Nandakumar

Poster 1: Divide And Concur the Scan World of Mammoth SoCs with Novel Pattern Porting Approach

Bharat Londhe, Akhtar Tamboli, Mayur Gavali, Pradeep Nagalapura

Poster 2: Debugging Scan Chain Hold Timing Violations with the Voltage BUMP Feature of ATE

Vinay Kumar and Bhrugurajsinh Chudasama

Poster 3: Generic methodology for emulation and test of a USB-PD Source

Shubha T R, Biju Erayamkot Panayamthatta and Mahadev G

Poster 4: Advanced Test Clock Generator (ATCG) to reduce the Pattern count and Improve the test Coverage

Shivasharanappa Biradar, Sneha Revankar and Abhinand Sk

Poster 5: An Adaptive Novel approach for SCAN Safety Sealing Checker in Pre-Silicon

Sudheer Anumala and Rajni Jain

Poster 6: Algorithm to translate natural language based test case to BDD based test case

Chandrashekhar Bhatta and Divya A L

Poster 7: Partition-level Boundary Scan re-use as is for SoC – shift left of Boundary Scan content bring up and validation

Prashant Sonone

Poster 8: Efficient Way of TPI for Pattern Optimization

Arindam Pratul Sarma, Deepen Talati and Savan Bhatelia

Poster 9: Droop compensation method in System Vmin measurement

Manjunath M R, Priyanka Sharma and Asaf Hay

Poster 10: Locating Faulty Memristors For Solving Sneak Path Problem in Memristive Crossbars

Aishwarya Deb, Subhadip Maji, Sanandita Das, Pooja Joshi and Hafizur Rahaman

Posters

Session Chair: Bharath Nandakumar

Poster 11: Enhanced DVS Flow for Attaining Highest Quality SoCs

Dharani Kumar Srinivasan, Mahesh Kumar M K and Praveen Raghuraman

Poster 12: On Board(IoB), ATE Solution & Implementation challenges for Ultra Low IB Measurements for Op-Amp

Aravind Lijoy and Bikash Gupta

Poster 13: An Area and Test-time Comparative Study On TAP and SIB based Networks In MBIST

Nadeem Pasha Mohammad, Mohit Mathur and Keerthana M

Poster 14: Securing the test infrastructure from FSA attack

M Prathiba and S Sivanantham

Poster 15: SOC Methodology for boundary conditions validation

Meghana L, Sreenivasa Rao Vuttaravilli and Tushar Jeevan

Poster 16: An Efficient Memory Grouping Methodology for MBIST

Tarun Goyal, Puneet Arora and Carl Wisnesky

Poster 17: ATPG driven masking of user-specified channels

Vaibhav Mishra, Aenikapati Swetha Priya, Sahil Narang, Bharath Nandakumar and Sameer Chillarige

Poster 18: Hierarchical Test Flow for Large SoC's

Vatsal Grover, Sarthak Singhal, Prashant Narang, Kapil Juneja and Khushboo Yadav

Poster 19: A comprehensive approach towards compact test pattern set generation for Small Delay Defects

Priyanka Bhatt, Leela Krishna Thota, Sreenivasarao Vuttaravilli and Sravan Kumar Challa

Poster 20: Burn-in and ATE Stress tests: Significance and Challenges in Post-Silicon Cycle

Abhishek Bhattacharya and Ananthashayana M S

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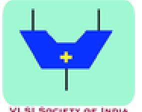

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