International Test Conference India 2023

IEEE International Test Conference, India 2023 - Agenda 23rd - 25th, July, 2023 Radisson Blu, ORR, Bangalore		
Tutorials		
Sunday, July 23, 2023		
8:00am-9:30am	**REGISTRATIONS**		
TRACKS	**TRACK 1** Session Chair | Santosh Kumar	**TRACK 2** Session Chair | Dr. Subhadip Kundu, Krishnamachary Prathapuram	**TRACK 3** Session Chair | Prof. R. Jayagowri
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
9:30 am - 11:00 am (15 mins. Break) 11:15 am - 12:45 pm	**Seamless Integration of packetized scan with Advanced ATE equipment** Lee Harrison (Siemens), Peter Orlando (Siemens), Michael Braun (Advantest) and Pudhukkarai Krishnan (Advantest)	**Design for Test – An indispensable slice of SOC (System on Chip) life cycle** Shamitha Rao, Bala Krishna K (Intel)	**DFX beyond Compression** Vijay Kumar K S, Kranthi Kandula, Leela Krishna Thota and Paras Chhabra (Synopsys)
12:45pm-1:45pm	**LUNCH BREAK**		
1:45 pm - 3:15 pm (15 mins. Break) 3:30 pm - 5:00 pm	**Error Resilient AI System: Addressing Soft Errors, Security, Threats and Manufacturing Variability Effects** Prof. Abhijit Chatterjee (Georgia Tech, USA) **Guaranteeing quality in automotive EMC tests through in-house EMC test** George Thottan, Rajesh Chauhan and Dilip Jain (Texas Instruments)	**Power Domains and Physical Synthesis – A DFT Perspective** Sarthak Singhal, Bharath Nandakumar, Subhasish Mukherjee and Dr. Krishna Chakravadhanula (Cadence) **Hierarchical and tile based DFT techniques for AI and Large SoCs** Lee Harrison and Peter Orlando (Siemens)	**Hardware Security: A perspective towards Fault Analysis Vulnerabilities** Prof. Bodhisatwa Mazumdar (IIT Indore) **Power Aware DFT** Karthik Natarajan, Likith Manchukonda, Manish Arora, Rahul Singhal and Greeshma Jayakumar (Synopsys)

	Conference - Day 1		
	Monday, July 24, 2023		
8:00am-9:15am	REGISTRATIONS		
9:00am-9:25am	Inauguration/Welcome | Sameer Chillarige, General Co-Chair, ITC India 2023		
9:25am-9:30am	Special Guests Talk , Ruchir Dixit (Siemens), Srinivas Chinamilli (Tessolve)		
9:30am-10:15am	**Keynote:** "Can Structural Test play a role in mitigating Silent Data Errors?", Dr. Nilanjan Mukherjee, Siemens		
10:15am-11:00am	**Keynote:** "Test industry challenges and solutions as observed by the leading physical implementation solution provider", Janet Olson, Cadence		
11:00am-11:30am	TEA/COFFEE BREAK SESSION		
SESSIONS	**Session 1 MBIST Test Challenges** Session Chair | Anuj Gupta	**Session 2 Productivity Enhancement through Improved Diagnosis** Session Chair | Veejaye Panayadian	**Session 3 AI/ML in Test** Session Chair | Jyotirmoy Saikia
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	1.1. Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation, Nikhil Karkare and Wilson Pradeep 1.2 MBIST-HSIO Concurrent Testing Strategies and Test Challenges, Boopala Krishnan, Shalini Mishra, Sumit Emekar, Subrahmanya M, Prasanna Ramanujam, Melvin Cu and Linfeng Pu 1.3 MBIST Area & Test Time Optimization Using Machine Learning Techniques, Darakshan Jamal and Ratheesh Thekke Veetil	2.1 A novel test data compaction method with improved debug capabilities of the signatures, Jaidev Shenoy, Kelly Ockunzzi and Dr. Virendra Singh 2.2 A novel approach to identifying scan issues during RTL validation, Alli Sravan, Malagiri Shashi Vardhan Reddy, Velamala Nithin and Ravathkar Ashwin Kumar 2.3 Addressing physically aware diagnosis challenges in hierarchical core based designs, Bharath Nandakumar, Sameer Chillarige, Robert C Redburn, Jeff Zimmerman and Nicholai L'Esperance	3.1 Application of Machine Learning in De-embedding of Signal Integrity Parameters for High Speed Serial Link, Maneesh Pandey, Mohit Goyal and Ajay Dash 3.2 Machine Learning Based MBIST Area Estimation, Puneet Arora, Virad Jain, Tarun Goyal and Norman Card 3.3 Hardware Simulator : Virtual Testing and Non-Product Failure Isolation, Akhila K, Shalini Srinivasan N, Gopikrishnan K and Harish G L
01:00pm-2:00pm	LUNCH BREAK		
SESSIONS	**Industry Session - 1** Session Chair | Shamitha Rao		**ART** Session Chair | Prof. Usha Mehta, Sandeep Jain
HALL NAME	GRAND VICTORIA		ARABICA & ROBUSTA
2:00pm-3:30pm	1. "Test Challenges in Known Good Die Chiplets based heterogeneous integration", Yogan Senthilkumar, Tessolve 2. "Advancements in Mixed-Signal Testing and Verification using Analog DFT Techniques", Prasanna Ramanujam, Qualcomm 3. "Silicon Life Cycle Management", Santosh Kumar, Synopsys		ART 1.1. Quality metric based optimal test option generation for small delay defects, M Prathiba and S Sivanantham ART 1.2. Lightweight Secured Split Test Technique with RMA Capability for Integrated Circuits, Sudeendra Kumar K, Akshay Girish Kaushik, Adithya B Shetty, Ashutosh Rao and Akshay S ART 1.3. Detection of hardware Trojans using Decision Tree Classifier at RTL of an ICs present in IoTs, Lavanya T and Dr Rajalakshmi K
3:30pm-4:00pm	TEA/COFFEE BREAK SESSION		
SESSIONS	**Panel Discussion** Session Chair | Kamlesh Pandey		**Poster Session** Session Chair | Bharath Nandakumar, Pranjal Giri
HALL NAME	GRAND VICTORIA		ARABICA & ROBUSTA
4:00pm-5:30pm	Voltage bump decisions to work around Vmin issues: are these based on any science or pure tribal art? 1.Jais Abraham (Qualcomm) 2.Srinivas Vooka (Google) 3.Prasad Mantri (AISemiCon) 4.Steve Palosh (Cadence) 5. Malav Shah (TI)		**Posters**

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	Conference - Day 2
	Tuesday, July 25, 2023
8:30am-9:15am	**REGISTRATIONS**
9:15am-9:30am	Welcome / Day 2 Summary | Kamlesh Pandey, General Co-Chair, ITC India 2023
9:30am-10:15am	**Keynote:** "Disruptive Technologies Drive a New Era of Test", Dr. Faadi Maamari, Synopsys
10:15am-11:00 am	**Keynote:** "Paradigm Shift: Structural Approaches to Analog and RF Test", Prof. Sule Ozev, Arizona State University
11:00am-11:30am	**TEA/COFFEE BREAK SESSION**

SESSIONS	Session 4 Power Aware DFT & Functional Test Session Chair | Raghu GG	Session 5 Advances in security Session Chair | Prof. Priyank Kalla	Session 6 Validation & Test Methodologies Session Chair | Jaidev Shenoy
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
11:30am-01:00pm	4.1 Power Domain Aware DFT Implementation, Sarthak Singhal, Subhasish Mukherjee, Christos Papameletis, Krishna Chakravadhanula, Ankit Bandejia, Dale Meehl, Archana Vyas and Mohan Gandla 4.2 Design of a Fault-Tolerant Pseudo-3D Routing, Biswajit R Bhowmik and Gagan N 4.3 Parallel Functional Test : A case study to reduce test cost in large SOCs, Akshatha P Inamdar, Syed Shadab and Karthik Chandrashekar	5.1 Invisible Scan for Protecting against Scan-based Attacks: You Can't Attack What You Can't See, Pravin Gaikwad, Patanjali Slpsk and Swarup Bhunia 5.2 Hidden in Plain Sight: A Detailed Investigation of Selectively Increasing Local Density to Camouflage and Robustify Against Optical Probing Attacks, Sajjad Parvin, Chandan Kumar Jha, Sallar Ahmadi-Pour, Frank Sill Torres and Rolf Drechsler 5.3 PROTECTS: Secure Provisioning of System-on-Chip Assets in Untrusted Testing Facility, Patanjali Slpsk, Jonathan Cruz, Sandip Ray and Swarup Bhunia	6.1 Scalable and Comprehensive approach for Concurrency Validation to improve Platform Stability, Naveena Nataraj, Jayaprakash Bs, Chockalingam A, Mandira Kumar Sathanantham, Kishore Chittudi, Ravishankar S, Abhishek Paliwal and Nihar Ranjan Saha 6.2 A formal approach to improve connectivity coverage in DFD, DFT, DFM, and DFX domain, Jayashri Patil, Kruttika Golwelker, Manu Yeeshu, Sood Surinder, Ananth Deepak K. S. and Shruti Deshpande 6.3 Prevention of High Current Events during Hot Testing at Turbo Frequency, Navaneeth A, Tiwari Himanshu, Sankapal Dudapa B and Vetcha Anand S
01:00pm-2:00pm	**LUNCH BREAK**		

SESSIONS	Industry Session - 2 Session Chair | Shamitha Rao	Session 7 Overcoming Analog/Mixed-Signal Test Challenges Session Chair | Prof. Sivanantham
HALL NAME	GRAND VICTORIA	ARABICA & ROBUSTA
2:00pm-3:30pm	1. "SSN - the next big thing", Lee Harrison, Siemens 2. "Mixed Signal Test - Challenges and Solutions", Nagarajan Viswanathan, Texas Instruments 3. Innovus Test Point - Enabling the next leap in coverage and test pattern reduction, Steve Palosh, Cadence	7.1 Analysis of Non-idealities in On-chip Loopback Testing of Data Converters, Tamajeet Mandal, Aswin R and Rubin Parekhji 7.2 Unified Analog Mixed-Signal Defect Simulation and Applications, Krishna Kumar Ganapathy Raman, Aswin R, Arshad Qureshi, Supraja R, Chanakya K V, Vijay Kumar Sankaran, Vinay Rawat, Victor Zhuk and Lakshmanan Balasubramanian 7.3 An SoC based Cost Effective Static Linearity Test Scheme for ADCs, P R R K Tirumalesu Manda and Keerthan Rai
3:30pm-4:00pm	**TEA/COFFEE BREAK SESSION**	

SESSIONS	Invited Talks Session Chair | Venkatarangam Totakura, Kavitha Shankar	Test Reality Check Session Chair | Vishal Vadhavania, Dimple Aggarwal
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4:00pm-5:30pm	1. Circuit Timing Marginalities and Silent Data Corruption, Prof. Adit Singh, Auburn University 2. Methodologies to evaluate Robustness of Modern Complex SoCs, Dr. Surya Musunuri, Infineon	TRC 1.1 HTOL Vector Utility(VecUtil) Tool For Protocol Aware Vectors, Boopala Krishnan, Shalini Mishra, Prasanna Ramanujam and Subrahmanya M TRC 1.2 Curious Case of Fab Process Variation on PLL Lock, Ajmal Firdous, Syed Feruz Syed Farooq, Himanshu Tiwari, Govil Badghare, Rucha Rathi and Kishore Kumar Banda TRC 1.3 Design/Manufacturing Challenges & Solution for highly Dense and large ATE DUT Boards, Rajiv Vk TRC 1.4 Novel Methodology to Optimize TAT and Resource utilization for ATPG Simulations for Large SoCs, Sudhakar Kongala, Anuj Gupta, Yash Walia and Sahil Jain
5:30pm-5:45pm	Closing Ceremony	