6th IEEE International Test Conference India 2022

24-26, July 2022

Venue: Radisson Blu, Bangalore, India

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Message from General Co-Chair

Sameer Chillarige, *Cadence*

General Co-Chair, ITC India 2022

*ITC India is all set to host the 6th edition of the conference from **July 24th – 26th 2022** at Radisson Blu, Bengaluru, India.*

The conference is back to in-person mode after 3 years with excellent keynotes, tutorials, technical papers, and panel discussions.

The keynotes and invited talks by technical experts and leaders cover all the major hot topics in test such as system level test, silicon analytics, 3DIC testing.

A special session on security by experts will cover effects of aging on security, security challenges in healthcare systems and techniques for detecting recycled ICs.

Starting this year, we are introducing short tutorials (90 minutes) along with full tutorials (180 minutes) to cover a bouquet of topics and also keep the contents focused.

We have planned 9 exciting tutorials that range from basics of test, DFT methodologies, analog testing, IEEE standards etc. to failure analysis challenges post silicon.

The panel discussion on Day 1 covers the challenges in of power aware testing and the Day 2 panel discussion deliberates on the burning problem of talent development in test domain.

There are many exciting technical papers planned along with a test reality check track that focuses on discussing day to day challenges faced by DFT engineers in the industry.

Starting this year, we are introducing a new academia track to provide a platform for PhD students in test/security domain to present their thesis and get invaluable feedback. A new mentorship program to help research students will be unveiled at the conference.

Review the agenda at https://itctestweekindia.org/itc-2022-agenda/ for the conference at https://itctestweekindia.org/register/ to participate, learn and get connected with the test and security community in industry and academia across the globe.

Looking forward to hosting you at the conference!!

Message from General Co-Chair

Kamlesh Pandey *Qualcomm India Pvt Ltd*

General Co-Chair, ITC India 2022

Finally, the wait is over as the 6th edition of ITC India is about to start in a few days (from July 24 to July 26) at Radisson Blu, Bangalore.

The products based on automotive and artificial intelligence are driving the growth of the modern semiconductor industry. These applications demand high quality, reliability, and security. Generally high-quality driven testing takes long test insertion, verification, and test application time, culminating into very high-test cost. Unfortunately, majority of the test time optimization techniques do not go hand in hand with low power testing techniques. The need of high reliability makes it necessary to detect latent defects using some voltage and/or temperature stress conditions. The over stress testing can potentially create walking wounded type of situation that affects long term reliability. The pressure of time to market does not provide any relief and mandates to have sophisticated diagnosis infrastructure for faster debug turnaround time. The concept of sophisticated diagnosis and idea of tight security are at loggerhead with each other. Finding optimum balance among quality, reliability, diagnosis, security and cost is a nontrivial task. These challenges make test faculty as one of the most challenging faculty of the modern-day VLSI industry.

As part of our commitment to proliferate test in academic institutions, we have included rich contents particularly carved out for students and faculties. The ITC provides an excellent opportunity to listen and interact with some of the best in the business test experts in the world. Please do visit ITC India 2022 home page to know more about agenda and registration details. Below are the agenda and registration links for a quick reference.

https://itctestweekindia.org/itc-2022-agenda/

https://itctestweekindia.org/register/

The ITC India organizing committee is looking forward to welcoming all the authors, presenters, panel members and audience to 6th edition of ITC India.

Message from Tutorials C0-Chairs



***Shamitha K**, Intel India*

***Dr.Subhadip Kundu,** Qualcomm India Pvt. Ltd*

***Dr. Sivanantham Sathasivam**, VIT, Vellore*

Welcome to the ITC India 2022!

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. At ITC India, design, test, and yield professionals can confront challenges faced by the industry, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers. This ITC India conference will be focusing on Test development in India but the submissions may not be limited to topics related to this region. Topics related to design and test development across multi geographical regions will be of special interest.

The Tutorials program at ITC India provides a spectacular platform to interact with industry veterans, gain in-depth understanding of topics from subject matter experts, honing problem-solving skills and challenge opinions. The ITC India conference is here to offer deep dive sessions on topics that range from the basics to the most advanced topics in the DFT world. The shorter version of tutorials , called 'Tutorial TitBits', is introduced to help reach greater depths of understanding , while the full versions cover the vastness of topics, thus reaching the breadth and depth of knowledge! This time we host 9 tutorials.

As always, we are looking forward to enthusiastic participation from all of you.

Message from Publication Co-Chairs

***Dr. Sivanantham Sathasivam**, VIT, Vellore*

***Dr.Sree Ranjani Rajendran**, University of Florida*

Welcome all of you to 6th IEEE International Test Conference India (ITC India 2022).

One of the primary goals of ITC India is to serve the professional and academic communities mainly of Indian subcontinent by presenting the highest quality technical program. At ITC India, design, test and yield professionals can confront challenges faced by the industry and learn how these challenges are being addressed by the combined efforts of academia, EDA tool and equipment suppliers, designers, and test engineers.

We express our gratitude to IEEE Bangalore section for supporting this event with financial co-sponsorship. As with last year, the ITC India 2021 proceedings will be available online through IEEE Explore and other scientific databases.

We thank the members of ITC India committee, IEEE, TTTC, IESA and VLSI Society of India for their diligence and dedication towards making this event a success.

We would also like to take this opportunity to thank *Technical Program Co-chairs* and all the external reviewers for their valuable efforts for making this conference a big success.

ITC India has been offering generous fellowships to students and teachers of various Indian academic institutions. The fellowship provides complimentary registration, Travel and Accommodation supports to attend all the Tutorials, Keynotes and Technical Sessions. This year 110 fellowships are awarded to the Faculty members, Research scholars and UG/PG students from Indian academic institutions across India to attend ITC India.

We are indebted to all the financial sponsors Qualcomm, Siemens, Intel, Synopsys, Tessolve Semiconductors, Cadence, Google and Texas Instruments for their generous contribution to ITC India 2022.

Let us plan to partake this banquet of knowledge and continue to march forward as a well-connected test community.

Looking forward to an enthusiastic participation from all of you!

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TUTORIALS 24 JULY 2022

	Sunday | 24 July, 2022		
8:00 am - 9:30 am	REGISTRATIONS		
TRACKS	TRACK 1 Session Chair | Dr. Subhadip Kundu	TRACK 2 Session Chair | Shamitha Rao	TRACK 3 Session Chair | Prof. Sivanantham S
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
9:30 am - 11:00 am (15 mins Break) 11:15 am - 12:45 pm	T1: Scan Test Escapes, New Fault Models, and Effectiveness of Functional System Level Tests Prof. Adit Singh (Auburn University)	T2: Basics of Design for Test – Enabling Manufacturing Test Sreekanth Pai and Balaji Upputuri (Marvell)	T3: Hierarchical DFT techniques for AI and Large SoCs Lee Harrison (Siemens)
		T4: Bridging the Gap Between Design-For-Test and Failure Analysis for Yield and Reliability Improvements Rakesh Kinger and Gaurav Mattey (Google)	T5: Challenges and Advances in Power-Aware Testing Dr. Ankush Srivastava (Qualcomm)
12:45 pm - 1:45 pm	LUNCH BREAK		
1:45 pm - 3:15 pm (15 mins Break) 3:30 pm - 5:00 pm	T6: A Complete DFT Methodology from Chip Planning to Implementation Niranjani Sukumar and Salvatore Talluto (Synopsys)	T7: Addressing Test, Safety and Security for Connected Automotive IC's Lee Harrison and Dr. Nilanjan Mukherjee (Siemens)	T8: Challenges of High Accuracy and Low-cost Test for Analog Power ICs, and the future Trends Gaurav Mittal (Texas Instruments)
			T9: Practical aspects of Implementing IEEE 1687 Rajesh Khurana and Dr. Vivek Chickermane (Cadence), Balaji Upputuri (Marvell)

CONFERENCE | DAY 1 25 JULY 2022

Monday | 25 July, 2022		
8:00 am - 9:15 am	REGISTRATIONS	
9:00 am - 9:25 am	Inauguration/Welcome | Sameer Chillarige, General Co-Chair, ITC India 2022	
9:25 am - 9:30 am	Special Guest Talk	
9:30 am - 10:15 am	Keynote 1: Meeting Testing challenges – An Integrated Approach, Jian Zhang, Qualcomm	
10:15 am - 11:00 am	Keynote 2: DFT to In-Life monitoring for dependable electronic systems, Ankur Gupta, Siemens EDA	
11:00 am - 11:30 am	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 1 - Advancements in Design For Test Session Chair | Dr. Ankush Srivastava	Session 2 - 3DIC test challenges & Advanced Fault Models Session Chair | Srinivasan Chandra Sekaran
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
11:30 am - 1:00 pm	1.1 Enhancing At-Speed Testability of Complex Inter-Core IO Interfaces, Wilson Pradeep, Muniswara Vorugu and Vevekanenda Gonugunta 1.2 Selective Multiple Capture Test (SMART) XLBIST, Peter Wohl, John Waicukauski, Anushree Bhat, Vijay Kumar K S and Rajit Karmakar 1.3 A novel fully automated multi-mode scan stitching architecture, Sarthak Singhal, Puneet Arora, Subhasish Mukherjee, Raghav Khemka and Krishna Chakravadhanula	2.1 TSV BIST Repair : Design-for-Test Challenges and Emerging Solution for 3D Stacked IC's, Akkapolu Sankararao, Vaishnavi G and Malige Sandya Rani 2.2 Accurate Diagnosis of Cell Internal Defects with Multiple Excitation and Propagation Conditions, Sonam Kathpalia, Sameer Chillarige, Bharath Nandakumar, Madhur and Santosh Malagi 2.3 An Efficient Test Time Model for Optimizing Tessent SSN for a 3D Design, Vasubabu Ravipati, Shyam N Kallepalli and Lance C Cheney
1:00 pm - 2:00 pm	LUNCH BREAK	
SESSIONS	Special Session - Security Session Chair | Subhasish Mukherjee	ART Track Session Chairs | Dr. Ankush Srivastava & Prof. Usha Mehta
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
2:00 pm - 3:30 pm	Recent Advancement in Detecting Recycled ICs, Prof. Ujjwal Guin, Auburn University Does Device Aging Affect Security?,	Analog, RF and mixed-signal IC Testing using AI enhanced alternate tests, Anshaj Shrivastava, IISc Bangalore

	Prof. Naghmeh Karimi, UMBC, USA Challenges in Design of Secure IoT based Industrial and Healthcare Systems, Prof. Susmita Sur-Kolay, ISI, India	Reliable and Fault-Tolerant Physically Unclonable Functions, Syed Farah Naz, IIT Jammu ML-Assisted Testing of Digital Circuits, Shruti Pandey, IIT Delhi Securing the test infrastructure of SoCs, Anjum Riaz, IIT Jammu Design of Efficient Programmable and Reconfigurable Pseudorandom Test Pattern Generator, Geethu R S, Amrita School of Engineering
3:30 pm - 4:00 pm	TEA/COFFEE BREAK SESSION	
SESSIONS	Panel Discussion - 1 Session Chair | Kamlesh Pandey	Poster Session Session Chair | Santosh Kumar & Bharath Nandakumar
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
4:00 pm - 5:30 pm	The Conundrum of Low Power Testing: Challenges, Solutions, and Associated Cost Panelists: 1. Dr. Rubin Parekhji (TI) 2. Prof. Adit Singh (Auburn) 3. Dr. Nilanjan Mukherjee (Siemens) 4. Gaurav Bhargava (Qualcomm) 5. Parthajit Bhattacharya (Synopsys)	Posters
5:30 pm - 6:30 pm	High Tea	

CONFERENCE | DAY 2 26 JULY 2022

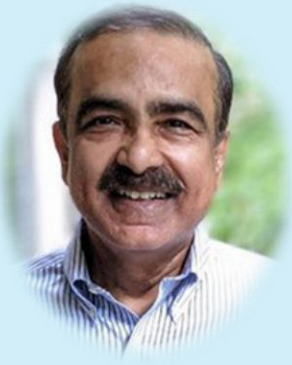
Tuesday | 26 July, 2022		
8:00 am - 9:15 am	REGISTRATIONS	
9:15 am - 9:30 am	Welcome / Day 2 Summary | Kamlesh Pandey, General Co-Chair, ITC India 2022	
9:30 am - 10:15 am	Keynote 3: Silicon Lifecycle Management: Trends, Challenges and Solutions, Yervant Zorian, Synopsys	
10:15 am - 11:00 am	Keynote 4: Convergence of SLT & ATE for SoC manufacturing test screening, Sajjad Pagarkar, Google	
11:00 am - 11:30 am	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 3 - Optimizations in Silicon Manufacturing & Test Application Session Chair | Srinivas Vooka	Session 4 - Test Methodology, Validation and Power Aware Test Session Chair | Bharath Nandakumar
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
11:30 am - 1:00 pm	3.1 Transfer-Matrix Abstractions to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits, Pratishtha Agnihotri, Priyank Kalla and Steve Blair 3.2 Towards Complete State Machine Traversal via Pseudo Transitions in Automated Lab Verification, Marc Huppmann, Manuel Harrant, Thomas Nirmaier, Andi Buzo, Linus Maurer and Georg Pelz 3.3 Implementation of Monotonicity Testing Utilizing On Chip Resources for Test Time Reduction, V Hemanthkumar	4.1 Test Methodology Automation for Multi-Die Package Realization, Durga Prasad Bade, Rohini Gulve, Adam Cron and Mike Ricchetti 4.2 Design of a programmable low power linear feedback shift register for BIST application, Maragathaeswari B and Geethu Remadevi 4.3 A System-Level Post-Silicon Validation Methodology for High-Speed Serial Interfaces, Sudeep Puligundla, Manikandan T, Paul Sunderland, Vineeth VI, Anshu Gupta, Felix Tudoran, Christopher Daffron, Moises Puga Nathal, Tim Linn, Wayne Huang, Saikiran V, Sukay Luhadia and Scott Gardiner
1:00 pm - 2:00 pm	LUNCH BREAK	
SESSIONS	TRC Track Session Chair | Anurag Jain & Vishal Vadhavania	Session 5 - Design for Security & Analog Test Session Chair | Prof. Jayagowri
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
2:00 pm - 3:30 pm	TRC 1 Enabling Hierarchical Assembly Build (MSIE) to improve turnaround time and performance for DFT pattern verification, Anuj Gupta, Sudhakar Kongala and Om Prakash Mishra	5.1 A Threshold based Hardware Trojan Detection Technique Using XGBoost Algorithm, Ranit Das, Tapobrata Dhar and Surajit Kumar Roy

	TRC 2 Enhanced Diagnosis on Scan and Memory Failures for 22ULL Tech Node, Arul Karthick Kumar, Vivek Roopchand and Balaji Duthae Srinivasan TRC 3 Validation Strategies to Achieve Zero Silicon bugs in DFT Logic, V N Sivakumar Avvaru, Souvik Sarkar, Prakash Kumar and Ashutosh Anand TRC 4 A Novel approach of improving test coverage using Z01X functional fault grading technique, Sreenivasa Rao Vuttaravilli, Leela Krishna Thota and Srinu Kona	5.2 Performance Enhancement of Unsupervised Hardware Trojan Detection Algorithm using Clustering-based Local Outlier Factor Technique for Design Security, S Meenakshi and Nirmala Devi M 5.3 Functional Testing of On-chip Analog/RF Circuits using Machine Learning based Regression Models, Anshaj Shrivastava and Gaurab Banerjee
3:30 pm - 4:00 pm	TEA/COFFEE BREAK SESSION	
SESSIONS	Invited Talks Session Chair | Kavitha Shankar	Panel Discussion - 2 Session Chair | Dr. C P Ravikumar
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
4:00 pm - 5:30 pm	1. Real Cost of Quality Based DFT, Punit Kishore, NXP 2. 3D stacked die (Foveros) technology: Concept, HVM test strategy and associated DFT, Shridhar Bendi, Intel	Talent Development in Test/Validation Domains Panelists: 1. Binoy Maliakal (TI) 2. Pathy Iyer (Keysight) 3. Rajesh Vaddempudi (Tessolve) 4. Prashant Narang (Cadence) 5. Venkat Sunkara (ChipEdge)
5:30 pm - 5:45 pm	Closing Ceremony	

Tutorial 1

Scan Test Escapes, New Fault Models, and the Effectiveness of Functional System Level Tests

PROF. ADIT D. SINGH (AUBURN UNIVERSITY)



Bio: *Adit Singh is James B. Davis Professor of Electrical and Computer Engineering at Auburn University, where he has served on the faculty since 1991. Earlier he has held faculty positions at the University of Massachusetts in Amherst, and Virginia Tech, in Blacksburg; and visiting professorships at the University of Freiburg, Germany, and the University of Tokyo, Japan. His research interests span all aspects of VLSI technology. He is particularly recognized for his pioneering contributions to statistical methods in test and adaptive testing. Dr. Singh has held leadership roles as General Chair/Co-Chair/Program Chair for dozens of VLSI design and test conferences and continues to serve on the Steering and Program Committees of many major international conferences in test and design automation. He served two terms (2007-11) as Chair of the IEEE Test Technology Technical Council (TTTC), and (2011-2015) on the Board of Governors of the IEEE Council on Design Automation (CEDA). Dr. Singh holds a B.Tech in Electrical Engineering from IIT Kanpur, and the M.S. and Ph.D. from Virginia Tech. He was elected Fellow of IEEE in 2002.*

Abstract:
This tutorial aims at understanding the increasing use of functional system level tests (SLTs) as an additional final defect screen before processor SOCs are shipped for assembly. For this, we take an in-depth look at traditional scan based Stuck-at and TDF tests to understand potential sources of test escapes. We also extensively discuss the effectiveness of new test generation methodologies such as Cell Aware, Gate Exhaustive, Transistor Stuck-Open, and Timing Aware in plugging these structural test holes. Based on this, we identify failures that can still remain undetected by low-cost scan structural tests, and require the use of expensive functional SLTs to achieve desired defect levels. In conclusion, we suggest strategies to minimize use SLTs without impacting defect levels.

Tutorial 2

Basics of Design for Test – Enabling Manufacturing Test

SREEKANTH G PAI AND BALAJI UPPUTURI (MARVELL)

Bio: *Sreekanth G Pai is a Principal Engineer, Design for Test in Central Engineering ASIC BU at Marvell India Pvt Ltd. Sree is currently leading end to end DFT implementation and validation on a customer chip while actively mentoring multiple DFT engineers to achieve DFT Execution Excellence. Sree has been a DFT Engineer for the past 10 years. His expertise ranges from creating best in class*

flows for DFT implementation/validation to defining and implementing custom DFT solutions to cater to Customer/Design needs and end to end DFT execution on complex customer designs. He joined Marvell India Pvt Ltd in 2019 through Avera Acquisition. He specializes in Hierarchical Test and Power Aware Testing. He has 2 filed patents along with multiple publications in technical forums such as ITC, VLSI-D, DAC, ISLPED, CDNLive.

Bio: *Balaji is currently working as Principal Engineer DFT, part of CE ASIC team. He has Joined Marvell in Nov2019 from Avera acquisition. He Has overall 16+ years of industry experience, Started VLSI journey from VEDAIIT Hyderabad after graduation in Electronics and communications from JNTU Hyderabad. He has started career with verification, FPGA and moved to DFT domain. Balaji has a wide set of expertise in DFT ranging from IP DFT, DFT implementation, PreSi Validation to Post-si debug. Currently, Balaji is focusing on defining DFT architecture solution for a 7nm and a 5nm complex network ASIC chips. He is adept at defining custom DFT solutions and his focus is to ensure First time right hardware. He holds 6 patents and 20 publications all of which are meaningful and relevant Innovations. Each of these ideas is highly impactful in improving Quality of Results and Turn Around time for DFT/Test solutions.*

Abstract:
This tutorial is intended to cover basic topics in DFT.
A list of topics that we plan to cover are as given below:

- An introduction to Manufacturing Test
- Yield, DPPM, Faults, Fault Models (10 mins)
- Introduction to Fault Models
- Basics of Scan based Testing
- Introduction to Scan Compression
- Introduction to ATPG Flow
- Simulations (with and without Timing annotation)
- Diagnosis (5 mins)

Tutorial 3

Hierarchical DFT techniques for AI and Large SoCs

LEE HARRISON (SIEMENS)

Bio: *Lee Harrison is Automotive IC Test Solutions Manager, with Mentor, A Siemens Business. He has over 20 years of industry experience with Mentor DFT products and has been involved in the specification of new test features and methodologies for Mentor customers, delivering high quality DFT solutions. With a focus on Automotive, Lee is working to ensure that current and future DFT requirements of Mentor's automotive*

customers are understood and met. Lee Received his BEng in MicroElectronic Engineering from Brunel University London in 1996.

Abstract:
The era of artificial intelligence (AI) and large chip designs has come. Cloud and infrastructure applications in AI are booming with new design architectures, methodology, technologies and design-for-test (DFT) requirements. CPU, GPU, FPGA, ASIC, DSP and many other technologies are used in large chips, which lead to many new architectures. We found it is very important for us to understand these new architectures and new technologies from both design and DFT point of view. This tutorial will cover the DFT challenges how a a range of technologies and a hierarchical approach can address these challenges.

Tutorial 4

Bridging the Gap Between Design-For-Test and Failure Analysis for Yield and Reliability Improvements

RAKESH KINGER AND GAURAV MATTEY (GOOGLE)

Bio: *Rakesh Kinger is currently responsible for DFT Productization tasks for consumer products silicon in Devices and Services (DSPA) group at Google. Rakesh has more than 25 years of hands-on experience in various areas related to Design-for-Test (DFT) implementation, silicon and system level test and debug, test quality, reliability and manufacturing. Before joining Google, Rakesh was responsible for leading DFT activities for complex network switching chips at Broadcom and for mobile SOCs at Qualcomm. Rakesh is the co-inventor for three US issued patents and has published multiple papers in international test and failure analysis related conferences. His areas of interest include Mixed Signal IPs testing, At-speed testing of SOCs, Memory and Logic*

Bio: *Since graduating with his Master's degree in Electrical Engineering-Solid State Electronics from the University of Michigan, Gaurav has 10+ years of experience in the Semiconductor industry specializing in Failure Analysis, Quality & Reliability, Yield bring-up, Scan/ATPG/MBIST Diagnosis, ATE based Test Engineering & Semiconductor Process Technology. Gaurav's role currently at Google Devices and Services (DSPA) group is that of NPI development Test Engineering Lead, responsible for ATE Test bring-up, Failure Analysis and DFT Diagnostics flow. Prior to joining Google, Gaurav worked as a Technical Lead for Microprocessor Product Development Engineering focusing on Failure Analysis & Yield bring-up for Mobile SOCs at Qualcomm and Graphics, Desktop and Server products at Advanced Micro Devices (AMD). Gaurav has published papers at international conferences and is also the co-author of a US issued patent in the fields of Test & Failure Analysis.*

Abstract:
Design for Testability (DFT) diagnosis and Failure Analysis (FA) play a very important role in identifying the key bottlenecks, especially during first silicon bring up in a new technology node. Effective diagnosis for both memory and logic defects help in identifying critical test, design marginality and process issues in a timely and efficient manner. However, as the process technology continues to scale and with increased design complexity, numerous challenges arise during FA. This tutorial covers the topic of bridging this gap between DFT implementation, diagnosis and FA so that some of these challenges can be met to ensure a very high success rate of identifying the defects. This tutorial will discuss different memory and logic defect diagnosis techniques along with any special requirements for DFT hardware and associated test modes and test patterns needed for facilitating FA. These techniques will be very instrumental in identifying critical criteria for FA candidate selection like the suspects/symptoms count, diagnostics score, physical proximity of suspects in layout, etc that would produce a high success rate. Electrical Fault Isolation (EFI) technique is selected depending on the type of failing pattern (Structural v/s Functional) and the parametric dependence (if any) of the failure across different voltage, frequency, temperature, etc. For advanced design debug on Automatic Test Equipment (ATE) and System Level Test (SLT) platforms, there are other sophisticated techniques used like Dynamic Laser Stimulation, Photon/Thermal Emission and Laser Voltage Probing/Imaging. Each of these techniques has its distinct test patterns and looping methodology requirements for compatibility with the associated FA tool. Such test-patterns need to be developed through close partnership with the DFT team. This tutorial will cover the details of such special test time optimized test patterns requirements like compression logic bypass, 1-hot chain patterns, PLL based trigger, etc. that enables EFI for FA. High quality and accurate fault isolation data drives downstream tools for physical FA (like nano-probing & TEM) that help to visualize the defects and/or identify process and design marginalities for feedback to foundry & yield learning. This effort will also help to dramatically reduce the number of costly physical failure analysis to identify systematic defects.

Tutorial 5

Challenges and Advances in Power-Aware Testing

DR. ANKUSH SRIVASTAVA (QUALCOMM)

Bio: *Ankush Srivastava is currently involved in enabling DFT methodologies for Qualcomm's state-of-the-art SoCs. He Has 15 years of industrial experience – Freescale/NXP/Qualcomm . He holds several international patents, journals and presented various papers in premier IEEE conferences. His current research interests include defining DFT architecture of complex SoCs, system security related to debug interfaces, effective and efficient small-delay defect-oriented test generation and low-power test methodology. He did his Ph.D. from IIT Bombay and M.E. from the BITS Pilani, all in Electrical Engineering. His Hometown is Lucknow and cycling is his hobby.*

Abstract:
The tutorial aims at understanding the issues of over-testing due to power supply droop during at-speed scan testing. The tutorial will start with the problem definitions and most recent solutions being offered either from the hardware designers or using CAD centric solutions. It will be proceeded by the pre-silicon and post-silicon hot-spot analysis with their respective effectiveness. At the end, we suggest effective strategies to minimize parametric yield loss due to over testing and possible efficient solutions available today.

Tutorial 6

A Complete DFT Methodology from Chip Planning to Implementation

NIRANJANI SUKUMAR, ADAM CRON, SALVATORE TALLUTO, RAHUL SINGHAL, HARISH K PRABHAKAR (SYNOPSYS)

Bio: *Niranjani Sukumar is a Solutions Manager at Synopsys in Hardware Analytics and Test group. Her current focus is on development of RTL based reference flows and reference methodologies. She had lead various methodology initiatives for gate level Scan flows. Niranjani received her MS (Micro Electronics) from Manipal University and BE (Electrical and Electronics) from Amrita Institute of Technology and Science.*

Bio*: Adam Cron is a Distinguished Architect at Synopsys working with customers worldwide on complex Security, DFT, and ATPG issues for SoCs. He is part of the Hardware Analytics and Test R&D group, and has been with Synopsys for over 24 years. Adam is helping to automate the implementation of secure silicon as part of the DARPA AISS program. Adam is Chair of IEEE Std 1838 which standardized 3D-IC test access, editor of IEEE Std P1149.4, and is an IEEE Golden Core recipient. He also chairs a working group creating a Rest API for MITRE's CWE and CAPEC databases.*

Bio: *Salvatore Talluto started in 1987 as an Asic Designer in Alenia Avionic Systems (currently Leonardo), he is now a DFT and Automation Architect in Synopsys, where he joined in 1998, supporting and developing DFT methodologies for major European customers, with focus on Automotive.*

Bio: *Rahul Singhal is a Product Manager for TestMAX DFT at Synopsys. His focus is the industry requirements and solutions in the areas of test compression, ATPG, and DFT for AI architectures. He developed and presented tutorial on DFT for AI chips and has co-authored multiple papers, posters on DFT and test in leading IEEE conferences. Rahul received his MS in Electrical Engineering from Portland State University and BS in Electrical Engineering from Purdue University.*

Bio: *Harish K Prabhakar is a Senior Staff Solutions Engineer at Synopsys. He began his career at Wipro and worked for Mindtree, Qualcomm & MediaTek before joining Synopsys. He has around 14 years of experience in VLSI industry working on Design for Testability (DFT). He has worked extensively on DFT implementation on multiple SoCs. Harish's current focus is on implementing Turnkey projects for customers spread across different geographies. He leads a team of engineers working on all fields of DFT. Harish has a Bachelor's degree in Electronics and Communication from Nehru College of Engineering & Research Centre under Calicut University*

Abstract:s

Growing demands of chips across multiple product segments and wide variety of complex architectures not only introduce challenges in chip design while it brings more challenges to Test. The challenges in DFT are seen across various disciplines such as clocking, power, performance, area, safety, security, reliability, in-system testing and so on. In this tutorial we introduce DFT implementation at RTL level with its benefits along with incremental low level synthesis-based DFT and cover the complete flow right from chip planning to implementation. We discuss the flow overview including planning and steps involved in taking care of various disciplines for DFT implementation and validation prior to DFT, during DFT and post DFT.

Tutorial 7

Addressing Test, Safety and Security for Connected Automotive IC's

Lee Harrison and Nilanjan Mukherjee (Siemens)

Bio: *Lee Harrison is Automotive IC Test Solutions Manager, with Mentor, A Siemens Business. He has over 20 years of industry experience with Mentor DFT products and has been involved in the specification of new test features and methodologies for Mentor customers, delivering high quality DFT solutions. With a focus on Automotive, Lee is working to ensure that current and future DFT requirements of Mentor's automotive customers are understood and met. Lee Received his BEng in MicroElectronic Engineering from Brunel University London in 1996.*

Bio: *Nilanjan Mukherjee is a Senior Director of Engineering for Tessent Silicon Lifecyle Solutions at Siemens EDA. He has been actively involved in the R&D of key technologies in the areas of test quality, test compression, Logic BIST, Memory BIST, low power DFT, and diagnosis. Some of his major accomplishments include being a co-inventor and an architect of EDT/TestKompress, the VersaPoint Test Points technology, a Low Power Hybrid EDT/Logic BIST scheme for automotive ICs, and the Observation Scan Technology (LBIST-OST). Currently, his focus is on developing new test solutions for automotive and data-center markets.*

Nilanjan has co-authored more than 85 technical papers and is a co-inventor of 55 US patents. He has received numerous awards including Best Paper Awards at VTS 2020, VLSI Design 2009, ATS 2001, and VTS 1995, the Most Significant Paper Award at ITC 2012, Siemens DISW Invention of the year 2019, and the Donald O. Pederson Outstanding Paper Award in 2006.

Nilanjan received a B.Tech. (Hons) degree from IIT, Kharagpur, and a Ph.D. degree from McGill University, Canada. He has given numerous tutorials, short-term courses, and invited talks at premier IEEE/ACM conferences, symposia, universities, and companies across the world.

Abstract:
This tutorial will focus on the expanding requirement and regulations surrounding test, safety and security for Automotive IC's. Looking at the various technologies and methodologies that can be used to address the different challenges and how these are being integrated to standardize and automate this process. We will deep dive into a wide range of different test and functional safety technologies, with a focus on traditional structural test and safety technologies, to more advanced system level testing IP used to collect operational data from the IC. We will also look at the security implications surrounding these technologies.

Tutorial 8

Challenges of High Accuracy and Low-cost Test for Analog Power ICs, and the future Trend"

GAURAV MITTAL (TEXAS INSTRUMENTS)

Bio: *Gaurav has 14 years of industry experience in analog test engineering. He is currently the test manager for Power Switching, Interface and Lighting business units at Texas Instruments, owning more than 5 investment areas for TI. He and his team focus on power protection and distribution devices across all analog market segments including automotive, industrial, PE, communication, and enterprise. He is the test architect for the group driving the test roadmap strategy, identifying the test gaps, and driving the systematic closure for them. Gaurav has a proven track record of self-sustaining test*

solutions and drove systematic cost, performance, and quality leadership at test, for these cost and quality-sensitive power devices. Since 2008, he has worked and defined test strategies across a variety of power devices including fuses, Hot-swap, LDO, ideal diode, current loop protectors, and high side drivers. Gaurav is a Member Group of Technical Staff (MGTS) at Texas Instruments since 2019. He has 14 papers (external and internal), 1 patent, an industry talk at the Asian test Symposium (ATS2019), and provided course lecture for VLSI test at IISc.

Abstract:
With high levels of integration using semiconductors, integrated circuits used for power monitoring and distribution (aka power ICs) face additional challenges from perspectives of transient protection, power dissipation and efficiency. The ATE production testing of these power ICs needs to deal with the contrarian trends of increasing load currents & accuracy requirements at one end, and shrinking ATE-error budgets & test costs at the other end. Specific test challenges include effective calibration of process-dependent parameters at high currents, reliable probe touchdowns against small pad size constraints, achieving low test costs using standard ATEs, improving measurement inaccuracies against poor thermals and self-heating at high currents, etc. Additionally, the use of such power ICs in automotive systems puts further demands on shipped product quality. The first segment of the tutorial will explain the recent trends in power ICs, roles & features, and these evolving challenges as mentioned above. It will also cover several test innovations to achieve these objectives, namely novel DFT implementations, test hardware solutions, and production test methodologies. The second segment of the tutorial will cover the ATE infrastructural challenges, overview & limitations of existing flows, and industry trends on newer ATE platforms. It will also describe the generic semiconductor manufacturing flow and packaging trends, providing broader perspectives on the challenges shown in the first segment. We shall wrap up the tutorial by discussing the future trends of Analog testing, quality aspects, and cost challenges. We shall also touch upon data analytics trends & adaptive testing on these devices, ATE co-simulation, and outlier detection trends.

Tutorial 9

Practical aspects of Implementing IEEE 1687

Rajesh Khurana, Dr. Vivek Chickermane (Cadence), Balaji Upputuri (Marvell)

Bio: *Rajesh is currently working as Director R&D at Cadence Design System, Noida, and leads a team working on IEEE 1687 & Low Power Tests. Prior to joining Cadence, he was Engineering Manager at Synopsis Bangalore office. He has over 25 years of experience spanning across multiple domains & technologies. His current interests are in Low Power Test methodologies and Embedded Macro Tests using IEEE 1687 and 1500. His contribution in the field of research includes five US patents and multiple publications at ITC (both India & US), ATS, NATW*

etc. He has master's in management and bachelor's in electrical engineering from DEI, Dayalbagh Agra.

Bio: *Balaji is currently working as Principal Engineer DFT, part of CE ASIC team. He has Joined Marvell in Nov2019 from Avera acquisition. He Has overall 16+ years of industry experience, Started VLSI journey from VEDAIIT Hyderabad after graduation in Electronics and communications from JNTU Hyderabad. He has started career with verification, FPGA and moved to DFT domain. Balaji has a wide set of expertise in DFT ranging from IP DFT, DFT implementation, PreSi Validation to Post-si debug. Currently, Balaji is focusing on defining DFT architecture solution for a 7nm and a 5nm complex network ASIC chips. He is adept at defining custom DFT solutions and his focus is to ensure First time right hardware. He holds 6 patents and 20 publications all of which are meaningful and relevant Innovations. Each of these ideas is highly impactful in improving Quality of Results and Turn Around time for DFT/Test solutions.*

Abstract:

The IEEE 1687 standard has rapidly gained popularity in the industry and is becoming the de facto method to deal with IP handoff and integration. IP developers can use the ICL and PDL files to describe their Instruments/IP blocks and the functional patterns, and these same files can be used by an EDA tool to re-target the functional tests to the SoC boundary. The 1687 standard inherently leverages the 1149.1 TAP interface for select, control and operation of a TDR within an Instrument, and has also found application in configuration of Hierarchal Tests and complex designs with LBIST and MBIST. This is even being used to control the turn/elevate inter-die logic for 3D Tests. This tutorial describes usage and application of 1687 and how it is being used to meet the Test and DFT requirements. It will cover how the IEEE 1687 standard can be used for retargeting of functional tests, configuration of Hierarchal Tests in presence of LBIST and MBIST, 3D Tests and explain the ICL and PDL languages, describe the most important constructs in the standard and how to use them. We will also discuss some of the advanced concepts like iMerge, Broadcast and Hierarchal SIB based designs which do not have sufficient explanation/examples in the standard.

KEYNOTES

Keynote 1

Meeting Testing challenges – An Integrated Approach

Jian Zhang, Qualcomm

Bio:

Jian is a semiconductor industry veteran with more than 25 years of experience in process technology development, foundry operations, product engineering. Jian has extensive experience in leading and integrating global teams from various regions and businesses, having spent more than a decade in the U.S. and Asia.

Jian is the Vice President in Qualcomm, leading the Product Test Engineering (PTE) in APAC, responsible for new product test development, characterization, and test deployment, yield management, integrating and optimizing performance for all products across the BUs. She also oversees technical and management coordination with the PTE teams in the U.S.

Prior to Qualcomm, Jian served as VP of technology at NXP, responsible for technology roadmap planning and execution, both for in-house fabs and foundries. She also partnered with foundry and internal teams to ensure all new products and foundry processes would meet the automotive quality requirements and work.

Jian held various management positions, including Global Foundries and Hewlett Packard. She holds master's and bachelor's degree in Electrical Engineering from Purdue University.

Abstract:

IC industry is in another "Golden Age", widely recognized for both strategic and commercial values. The powerful drive towards intelligent connected world, real and virtual, puts unprecedented demands on faster, better, affordable products. Transition to heterogeneous integration and leading edge technologies pose further challenges in product testing – in areas of DFT, Diagnosis, In-Test Thermal/Power Management to name a few. Automotive quality requires new thinking in test for margin. An integrated approach, starting with meticulous DFT & EDA solutions architected upfront, coupled with quick learning from Terabytes of Testing Data, is needed to solve tomorrow's problem. We, at Qualcomm continue to be excited about the future of DFT & Test opportunities in the days ahead.

Keynote 2

DFT to In-Life monitoring for dependable electronic systems

Ankur Gupta, Siemens EDA

Bio:

Ankur Gupta is Vice President and General Manager of Tessent Test and Embedded Analytics business at Siemens EDA. Formerly he was head of Product Management and Applications at Ansys, Semiconductor and Head of Applications Engineering for Digital Implementation & Signoff at Cadence Design Systems. Ankur has 20+ years of experience in EDA, working on some of the industry's most innovative Digital Design, Implementation and Signoff products. He holds 4 US Patents and a Master's Degree in Electrical and Computer Engineering, from Iowa State University.

Abstract:

The reliable and secure operation of electronics, i.e., healthy electronics, in safety-critical, enterprise servers and cloud computing domains is a major challenge. Traditionally, manufacturing test solutions were intended to guarantee the in-life reliability and security of electronic systems. However, as the diversity and complexity of software workloads drive huge increases in the complexity of these systems, unexpected inefficiencies, anomalies, and vulnerabilities cause outsized effects on the end application. This is a drag on business performance. Therefore, the solutions for in-life management need to extend beyond robust design-for-test. Sensors and monitors must be embedded in different levels of the design stack, providing both structural and functional views of the system, with a solution that is built on a foundation of strong industry leading products and industry standard access mechanisms as well as data analytics that run on the edge and in the cloud. To drive successful business outcomes, the industry must consider investing in key technology components, including trusted design-for-test platform, silicon-proven functional monitors and analytics that deliver actionable outcomes.

Keynote 3

Silicon Lifecycle Management: Trends, Challenges and Solutions

Yervant Zorian, Synopsys

Bio:

Dr. Yervant Zorian is a Chief Architect and Fellow at Synopsys, as well as President of Synopsys Armenia. Formerly, he was Vice President and Chief Scientist of Virage Logic, Chief Technologist at LogicVision, and a Distinguished Member of Technical Staff AT&T Bell Laboratories. He is currently the President of IEEE Test Technology Technical Council (TTTC), the founder and chair of the IEEE 1500 Standardization Working Group, the Editor-in-Chief Emeritus of the IEEE Design and Test of Computers and an Adjunct Professor at University of British Columbia. He served on the Board of Governors of Computer Society and CEDA, was the Vice President of IEEE Computer Society, and the General Chair of the 50th Design Automation Conference (DAC) and several other symposia and workshops.

Dr. Zorian holds 35 US patents, has authored four books, published over 350 refereed papers and received numerous best paper awards. A Fellow of the IEEE since 1999, Dr. Zorian was the 2005 recipient of the prestigious Industrial Pioneer Award for his contribution to BIST, and the 2006 recipient of the IEEE Hans Karlsson Award for diplomacy. He received the IEEE Distinguished Services Award for leading the TTTC, the IEEE Meritorious Award for outstanding contributions to EDA, and in 2014, the Republic of Armenia's National Medal of Science.

He received an MS degree in Computer Engineering from University of Southern California, a PhD in Electrical Engineering from McGill University, and an MBA from Wharton School of Business, University of Pennsylvania.

Abstract:

Recent growth in utilizing AI Accelerators, in data centers and automotive SOCs have led to an explosion in the adoption of emerging technology nodes and 3DIC/chiplet packages. This keynote will first present today's trends, then concentrate on resiliency challenges for such emerging SOCs, and then will discuss optimizing their health using advanced solutions, which are typically utilized for managing all the silicon lifecycle stages: from silicon debug in early bring up stage to shorten the time-to-market; to self-test and repair during volume production stage to improve quality and yield; to power-on self-test in the field to address aging defects; to in-system periodic checking in the field to improve functional safety; and finally to fault tolerance and error correction during the mission mode to address a range of transient errors. All of the above are realized by on-chip and off-chip data analytics.

Keynote 4

Convergence of SLT & ATE for SoC manufacturing test screening

Sajjad Pagarkar, Google

Bio:

Sajjad Pagarkar is Head of Post Silicon Engineering in the Core Technology Division at Google. He has led Product development and test engineering teams of numerous complex SoC's in the past 22 years, enabling shipping of billions of mobile & compute chips. For the last 10 years Sajjad has extensively worked on development of SLT from ground zero to massively parallel screening solutions to enable high volume productization of SOC's from 16nm down to 4nm technologies. When Sajjad is not at his desk, you can find him hiking in the woods of his home state, California.

LinkedIn: *https://www.linkedin.com/in/sajjad-pagarkar-7b0b525/*

Abstract:

The outgoing quality requirement & time to high volume production of today's mobile/compute/AI SoC are significantly tighter than those for the conventional SOC's. Bringing products with shorter time to market with low DPPM in latest semiconductor process technology nodes have created many challenges in DFT & post silicon high volume production screening domains. We need a very sound test strategy to manage low outgoing DPPM with optimum cost of test. The unique challenges associated with productization of mobile/compute/AI SOCs will be addressed in the talk, along with our experience in overcoming them.

PANEL DISCUSSION 1

THE CONUNDRUM OF LOW POWER TESTING: CHALLENGES, SOLUTIONS, AND ASSOCIATED COST

Abstract: The significant growth of the wireless and portable devices is driving deployment of sophisticated power reduction techniques in the mission mode. At the same time, shrinking technology nodes and demand for high quality are mandating use of advanced fault models, resulting in massive test data volume. Moreover, compact test pattern sets cause maximum toggle activities and hence not suitable for low power testing. To keep test time under control, techniques such as testing multiple cores together or increasing frequency of test clocks are deployed. All these measures increase test power consumption and cause yield loss. To circumvent yield loss issue, commonly used measures are voltage boost, low toggle ATPG patterns or serialized core testing. The panel will discuss low power testing challenges, available solutions, and associated cost.

1. *What are the low power test challenges?*
2. *What are the various techniques used to contain power during Logic Testing?*
3. *What are the various techniques used to contain power during Memory testing?*
4. *Do we have good pre silicon test power estimation tools and processes?*
5. *How to account for glitch power?*
6. *Thoughts on impacts of global IR drop and local IR drop.*
7. *Do we need to be concerned about L di/dt?*
8. *Is applying voltage boost a correct strategy to improve yield and reduce test time?*
9. *Does voltage boost mask effects of some real defects?*
10. *Thoughts on testing low power instruments like power switches, isolation cells etc.*
11. *Thoughts on future measures to address low power testing issues.*

Panelists:

Rubin Parekhji (TI)

Adit Singh (Auburn)

Nilanjan Mukherjee (Siemens)

Gaurav Bhargava (Qualcomm)

Parthajit Bhattacharya (Synopsys)

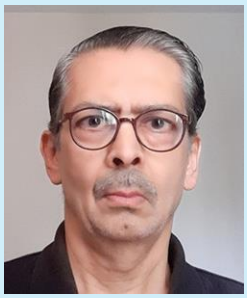
Moderator: Kamlesh Pandey (Qualcomm)

Moderator Details

Kamlesh Pandey (Qualcomm)

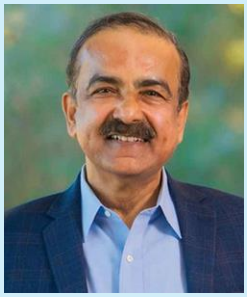
Kamlesh Pandey is a Director, Engineer at Qualcomm India Pvt Ltd. He joined Qualcomm Bangalore in 2021. He is currently leading ATPG vertical of BDC DFT group. Prior to joining Qualcomm, he has worked at Broadcom India Pvt Ltd for 17 years and his last designation at Broadcom was Distinguished Engineer. At Broadcom he led a team working on DFT architecture, DFT flow development, DFT implementation on SOCs, ATE bringup and production support for Settop box and DOCSIS SOCs. Prior to joining Broadcom, he was DFT engineer at Cisco Systems. His contribution in the field of research includes multiple US patents and invention of Broadcom in-house at-speed logic test architecture known as CTSA. He has received M.Tech. in Microelectronic and VLSI systems from Indian Institute of Technology Kanpur.

Panelist Details



Rubin Parekhji (TI)

Rubin Parekhji has been with Texas Instruments (India), Bangalore, since 1996, where he has led and mentored DFT teams on various IP / SOC design and test technology projects across multiple groups, resulting in many DFT and test innovations, and adoption of new test technologies across TI teams world-wide. He has co-authored more than 70 peer reviewed technical papers and has contributed to more than 20 tutorials and special sessions in leading international conferences. He has played chair roles in IEEE conferences and standards. He has been a visiting faculty member at IIT Bombay and IISc Bangalore, has guided a large number of students on industrial projects, and is an active liaison for several TI sponsored SRC projects. He is the joint inventor of 25 granted patents and is a distinguished member of technical staff at TI. He has a Ph.D. from Indian Institute of Technology, Bombay, India.



Adit Singh (Auburn)

Adit Deva Singh is Godbold Endowed Chair Professor of Electrical and Computer Engineering at Auburn University, where he has served on the faculty since 1991. Earlier he has held faculty positions at the University of Massachusetts and Virginia Tech, in Blacksburg, and visiting professorships at the University of Freiburg, Germany, and the University of Tokyo, Japan. His research interests span all aspects of VLSI technology, with an emphasis on IC test and reliability. Professor Singh has held leadership roles as General Chair/Co-Chair/Program Chair for dozens of VLSI design and test conferences, including on the steering committee of ITC. He helped co-found the International Conference of VLSI Design in India in 1990-91. For two terms (2007-11), he was Chair of the IEEE Test Technology Technical Council (TTTC), and also served (2011-2015) on the Board of Governors of the IEEE Council on Design Automation (CEDA). He holds a B.Tech in Electrical Engineering from IIT Kanpur, and the M.S. and Ph.D. from Virginia Tech. He is a Life Fellow of IEEE.

Nilanjan Mukherjee (Siemens)

Nilanjan Mukherjee is a Senior Director of Engineering for Tessent Silicon Lifecyle Solutions at Siemens EDA. He has been actively involved in the R&D of key technologies in the areas of test quality, test compression, Logic BIST, Memory BIST, low power DFT, and diagnosis. Some of his major accomplishments include being a co-inventor and an architect of EDT/TestKompress, the VersaPoint Test Points technology, a Low Power Hybrid EDT/Logic BIST scheme for automotive ICs, and the Observation Scan Technology (LBIST-OST). Currently, his focus is on developing new test solutions for automotive and data-center markets.

Nilanjan has co-authored more than 85 technical papers and is a co-inventor of 55 US patents. He has received numerous awards including Best Paper Awards at VTS 2020, VLSI Design 2009, ATS 2001, and VTS 1995, the Most Significant Paper Award at ITC 2012, Siemens DISW Invention of the year 2019, and the Donald O. Pederson Outstanding Paper Award in 2006.

Nilanjan received a B.Tech. (Hons) degree from IIT, Kharagpur, and a Ph.D. degree from McGill University, Canada. He has given numerous tutorials, short-term courses, and invited talks at premier IEEE/ACM conferences, symposia, universities, and companies across the world.

Gaurav Bhargava (Qualcomm)

Gaurav Bhargava is a Sr. Director, Technology at Qualcomm India Pvt Ltd. He is responsible for DFT Test Productization in High Volume Manufacturing for Qualcomm's Snapdragon product lines. In his 20-year career with Qualcomm (USA & India), Gaurav has contributed within various fields of Test – ranging from Pre-Silicon Test Architectures, DFT Implementation & Fault Modelling to Post-Silicon Test Development & Product/Test Engineering. He has seen SoC Designs & Semiconductor Test evolve from the early 130nm era to the current 3nm where he actively contributes towards Yield, Quality, Reliability & Test-Cost Goals across product lines. He holds multiple patents in DFT and has published several papers in leading Semiconductor Test Conferences globally. Gaurav earned his bachelor's degree in Electronics Engineering from University of Mumbai and holds a master's degree in Computer Science & Engineering from State University of New York, Buffalo, USA.

Parthajit Bhattacharya (Synopsys)

Parthajit Bhattacharya is a Director R&D, at Synopsys. Working with Synopsys since 2008, leading a team of excellent engineers who are developing cutting edge technologies in TestMAX family of products. Collaborating with esteemed customers on various aspects of DFT and ATPG, addressing critical test issues and enabling effective test for the most demanding applications. Interested in learning and collaborating on new technology for solving current and future challenges in VLSI Test.

PANEL DISCUSSION 2

TALENT DEVELOPMENT IN TEST/VALIDATION DOMAINS

Abstract: The International Test Conference (India) is an excellent platform to discuss a practical *problem that challenges semiconductor companies based in India, namely, the problem of talent acquisition and retention, especially in the areas of test and validation. A number of companies recruit engineers without the relevant background and provide on-the-job training. Not only is this expensive, it is not sustainable in the long run. On-the-job training is a short-term solution. Highly talented individuals who need to make a career in the test and validation area look for a good theoretical foothold, which is best provided as part of academic education. I propose to have a panel discussion on the topic of talent development in the test and validation domains, where panelists will debate on practical issues facing the industry and academic institutions, and offer some solutions to overcome these problems.*

Panelists:

Binoy Maliakal (TI)

Pathy Iyer (Keysight)

Rajesh Vaddempudi (Tessolve)

Prashant Narang (Cadence)

Venkat Sunkara (ChipEdge)

Moderator: Dr C P Ravikumar

Moderator Details

Dr C P Ravikumar

C.P. Ravikumar has 23 years of experience in the industry (Texas Instruments, Controlnet India, and Infosys). I also have 10 years of teaching experience at IIT Delhi. I obtained my Ph.D. from the University of Southern California. More personal information about me is available from cpravikumar.tripod.com. As a secretary of the VLSI Society of India and IEEE CAS Bangalore, I have organized hundreds of workshops, seminars and tutorials. I have been the General Chair and Program Chair of premier events such as the International Conference on VLSI Design and I initiated the VLSI Design and Test Symposium and nurtured it for 16 years as its Generaal Chair. I have conducted more than 25 panel discussions in different conferences. I have also participated as a panelist in a few panel discussions.

Panelists Details

Binoy Maliakal, Texas Instruments

Binoy Maliakal has 33+ Years in Semiconductor Fab, Product, Test and Validation Engineering, 11yrs in Semiconductor Wafer Fab and Integrated Circuits Test at Bharat Electronics (BEL) and 16yrs in Test, Validation and Product Engineering at Cypress Semiconductor (Infineon now).
Last 6yrs in Texas Instruments. Engineering Director of Product, Test and Validation in Analog Power Products Team.

Pathy Iyer, Keysight

- Head, Business Development at Keysight
- Has helped many Universities in setting up labs and define curriculum in Test/RF
- Skilled in Product Marketing, Product Development, Research and Development (R&D), Cross-functional Team Leadership, and Electronics.
- Strong consulting professional.

Rajesh Vaddempudi, Tessolve

- 22+ years of experience in Test and Product Engineering across products (PMIC / Mixed Signal / HSIO etc) and across ATE platforms.
- Presently leading 1000+member Test Product Engineering team at Tessolve as Vice President Test Engineering.
- Part of the leadership team to grow Test product engineering expertise across multiple locations of Tessolve and provide quality test solutions to customers.
- Passionate about training and grooming local talent and producing low-cost test solutions to support volume manufacturing.

Prashant Narang, Cadence

• Prashant Narang is Product Validation Director of Test team at Cadence with 20 years of industry experience.
• He has received several awards for significant improvement in process, quality and operational excellence.
• He was General chair of Technology and Quality Conference i.e. TEQfest at Cadence in 2019.

Venkat Sunkara, ChipEdge

- 22 yrs experience in Semiconductor industry
- Founded Chipedge in 2012 and offering skill development courses in VLSI for last 10 years including a course in DFT.

INVITED TALKS

Recent Advancement in Detecting Recycled ICs

Ujjwal Guin, Auburn University

Bio:

Ujjwal Guin is currently an Assistant Professor at the Department of Electrical and Computer Engineering, Auburn University. He received his Ph.D.degree from the University of Connecticut in 2016. He is actively involved in projects in the field of Hardware Security and Trust, Supply Chain Security, Cybersecurity, and VLSI Design and Test. He has developed several on-chip structures and techniques to improve the security, trustworthiness, and reliability of integrated circuits. His current research interests include Hardware Security & Trust, Blockchain, Supply Chain Security, Cybersecurity, and VLSI Design & Test. He is a co-author of the book "Counterfeit Integrated Circuits: Detection and Avoidance". He has authored several journal articles and refereed conference papers. His projects are sponsored by the National Science Foundation (NSF), Air Force Research Laboratory (AFRL), and Auburn University.

Prof. Guin was actively involved in developing a web-based tool, Counterfeit Defect Coverage Tool (CDC Tool), http://www.sae.org/standardsdev/cdctool/. This tool has been adopted in "AS6171: Test Methods Standard; General Requirements, Suspect/Counterfeit, Electrical, Electronic, and Electromechanical Parts" for the basis of test method selection and evaluation of test effectiveness.

He serves on organizing committees of HOST, VTS, ITC-India, and PAINE. He is on the technical program committees in several reputed conferences, such as DAC, HOST, ITC, VTS, PAINE, VLSID, GLSVLSI, ISVLSI, and Blockchain. He serves in the SAE International G-19A Test Laboratory Standards Development Committee and G-32 Cyber-Physical Systems Security Committee. He is a member of both the IEEE and ACM.

Abstract:

The continuous growth of counterfeit integrated circuits (ICs) in the electronics supply chain calls for an immediate solution as their inferior quality poses serious threats to our critical infrastructures. Information Handling Services Inc. reported that counterfeit ICs represent a potential annual risk of $169 billion to the global electronics supply chain, and the trend continues. Among all counterfeit categories, recycled ICs account for almost 80% of all reported counterfeit incidents. Deploying these recycled chips in critical infrastructure would be catastrophic as they exhibit lower performance and shorter lifespan than a newly manufactured IC. In addition, the crude recycling process of removing ICs from printed circuit boards (PCBs) under extremely high temperatures, followed by sanding, repackaging, and remarking, could potentially create additional defects and anomalies. Moreover, the recycling process may also create latent defects. Although a counterfeit IC may pass the initial acceptance testing by original equipment manufacturers (OEM), it is susceptible to failure in the field.

In this presentation, we first present a robust and low-cost solution for enabling the traceability of an IC. The proposed solution builds a chain of trust among the manufacturer, distributors, and system integrator by providing endto-end traceability in the semiconductor supply chain and protecting against IC recycling. The proposed solution utilizes a small passive radio-frequency identification (RFID) tag, which needs to be placed on the package. Any supply chain entity can verify a chip's authenticity using a commercial RFID reader.

Second, we present a novel approach to estimating the operational age of ICs by measuring IDDQ, the quiescent current from the power supply, or the total leakage current in steady-state. This current decreases as the circuit ages, largely due to the increase in the magnitude of the PMOS transistor threshold voltage caused by negative bias temperature instability (NBTI). The impact of NBTI on PMOS transistors depends upon the operational stress, that is, the duration of its ON state. Our technique uses the normalized difference, ΔI, computed from current measurements at two input test patterns, as the self-referencing circuit age indicator. The first pattern is chosen such that its IDDQ is controlled by a large number of minimally stressed PMOS transistors. As for the second pattern, the IDDQ is controlled by an approximately equal number of highly stressed PMOS transistors. The difference between these two IDDQ values increases as the circuit ages. This approach requires no hardware modification in the circuit and can be applied even to legacy ICs.

Finally, we show a new and highly effective approach for detecting recycled ICs by exploiting the power-up state of on-chip SRAMs. Our methodology does not require the introduction of any special aging detection circuitry nor a record of historical circuit performance data as its reference. Instead, we exploit the power-up state of an SRAM with an equal number of cells power up to the 0 and 1 logic states to detect prior usage. Since SRAMs exist in virtually all system-on-chips (SoCs), this simple aging detection method can be applied to chips already circulated in the market.

Does Device Aging Affect Security?

Naghmeh Karimi, UMBC, USA

Bio:

Naghmeh Karimi received a Ph.D. degree in Computer Engineering from the University of Tehran in 2010. She was a visiting researcher at Yale University, USA between 2007 and 2009, and a post-doctoral researcher at Duke University, USA during 2011-2012. She has been a visiting assistant professor at New York University and Rutgers University between 2012 and 2016. She joined the University of Maryland Baltimore County as an assistant professor in 2017 where she leads the SECure, REliable and Trusted Systems (SECRETS) research lab. She has published three book chapters and authored/co-authored more than 70 papers in refereed conference proceedings and journal manuscripts. She is a senior member of IEEEm and serves as an Associate Editor of the Springer Journal of Electronic Testing: Theory and Applications (JETTA) and IEEE Design \& Test Journal. She has been the corresponding guest editor of the Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS); special issue in Hardware Security in Emerging Technologies in 2021. Her current research interests include hardware security, VLSI testing, design-for-trust, design-for-testability, and design-for-reliability. She is a recipient of the National Science Foundation CAREER Award in 2020.

Abstract:

With the aggressive scaling of VLSI technology, aging-related degradation of integrated circuits has received a lot of attention. Aging changes the specifications of transistors during the time and in turn, the timing and power consumption of the underlying devices. Thereby, agingrelated degradations can affect the success of the physical attacks targeting cryptographic cores through power side-channel attacks or fault injection attacks in order to leak sensitive data. In this presentation, we discuss the aging-induced security concerns in cryptographic devices and show how the security is diminished for some of these physical attacks when the device is aged. We also discuss the countermeasures we developed to provide long-lasting security against such attacks.

Challenges in Design of Secure IoT based Industrial and Healthcare Systems

Susmita Sur-Kolay, ISI, India

Bio:

Susmita Sur-Kolay has been a faculty at the Indian Statistical Institute and is presently a Senior Professor. She was the Professor-in-Charge of the Computer and Communication Sciences Division of ISI till 2018. She received the B.Tech. degree in electronics and electrical communications engineering from IIT Kharagpur, and the Ph.D. degree in computer science and engineering from Jadavpur University. She was in the Laboratory for Computer Science at Massachusetts Institute of Technology for as a Graduate Research Assistant, a Postdoctoral Fellow at the University of Nebraska–Lincoln, a Reader at Jadavpur University during 1993-1999. She was a Visiting Faculty Member at Intel Corporation, USA in 2002,and a Visiting Researcher at Princeton University in 2012. Her research contributions are in the areas of algorithms for design automation of secure electronic systems and reliable quantum computers, graph algorithms. She has co-authored edited books, several technical papers in leading international journals and refereed conference proceedings, a chapter in the Handbook on Algorithms for VLSI Physical Design Automation. She has served on the committees of many international conferences and Editorial boards of leading journals. She was a Distinguished Visitor (India) of the IEEE Computer Society, an Associate Editor of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems and ACM Transactions on Embedded Computing Systems. She is a Fellow of Indian National Academy of Engineering, among other awards a recipient of the President of India Gold Medal and a Distinguished Alumnus Award of IIT Kharagpur, Women in Technology Leadership Award of the VLSI Society of India.

Abstract:

Internet of Things (IoT), also referred to as the Internet of Objects, is transforming the approach for providing numerous services. Compact and portable lightweight smart devices are an essential part of IoT. They range widely in use, size, energy capacity, and computation power. However, the integration of these smart things into the standard Internet introduces several security challenges because the majority of Internet technologies and communication protocols were not initially designed to support IoT. Moreover, commercialization of IoT has led to public security concerns, including personal privacy issues, threat of cyber attacks, and organized crime. In order to provide a guideline for those who want to investigate IoT security and contribute to its improvement, a comprehensive list of vulnerabilities is provided first along with suitable countermeasures against them.

Most IoT initiatives in healthcare revolved around the improvement of care as such with remote monitoring and telemonitoring as main applications. Wearable medical sensors (WMSs) are garnering ever-increasing attention from both the scientific community and the industry. Driven by technological advances in sensing, wireless communication, and machine learning, WMS-based systems have begun transforming our daily lives.

A second area where many initiatives exist is tracking, monitoring and maintenance of assets on the level of medical devices and healthcare assets, the people level and the non¬medical asset level (e.g. hospital building assets). These deployments are just the beginning and, at the same time, are far from omnipresent. More advanced and integrated approaches within the scope of the digital transformation of healthcare are starting to be used with regards to health data aspects where IoT plays an increasing role, as it does in specific applications such as smart pills, smart home care, personal healthcare, robotics and Real¬Time Health Systems (RTHS).

Notwithstanding all these benefits, Information security has become an important concern in healthcare systems, owing to the increasing prevalence of medical devices and the growing use of wearable and mobile computing platforms for health and lifestyle monitoring. Early works in the area of health information security has largely focused on attacks on the wireless communication channel of medical devices, or on health data stored in online databases. Recent works have also addressed entirely different angles to health information security being motivated by the insight that the human body itself is a rich source (acoustic, visual, and electromagnetic) of data.

Although WMSs were initially developed to enable low-cost solutions for continuous health monitoring, the applications of WMS-based systems now range far beyond health care. Several research efforts have proposed the use of such systems in diverse application domains, e.g., education, human-computer interaction, and security. Even though the number of such research studies has grown drastically in the last few years, the potential challenges associated with their design, development, and implementation are neither well-studied nor well-recognized.

This lecture presents first the different aspects of IoT security and then a couple of scenarios depicting the potential risks. Next, the desiderata for secure healthcare IoT system design are discussed in general, followed by possible cases of inadvertent information leakage. Finally, energy efficiency of health monitoring is addressed and how applications of healthcare IoT systems beyond health monitoring can be built is described.

Real Cost of Quality Based DFT

Punit Kishore, Senior Director (NXP)

Bio:

Punit received his B. Tech. (EE) from IIT Kanpur in 2004. He is currently Senior Director, DFT at NXP Semiconductors. He currently drives global DFT architecture and Product execution for MCU-MPU Engineering organization. Prior to NXP, he has worked for Texas Instruments, NVIDIA, Intel and Qualcomm. Punit has worked in different aspects of DFT like ATPG, diagnosis, mixed signal DFT, memory testing and repair, IO-DFT, CAD, Methodology development etc. He has worked extensively in defining automotive DFT architecture for ADAS and accelerator chips at Qualcomm. He has also managed SOC execution as design manager role at Qualcomm. He holds 7 USPTO granted patents in the field of DFT. He has pioneered USB based testing of SOC at industry level.

Abstract:
A framework for assessing the cost of semiconductor device manufacturing and the role of DFT engineering in achieving quality tradeoffs. NXP plays in a very diverse eco-system, where there is varied quality requirement, a case study will be presented to substantiate the framework. This talk will cover architectural elements, device physics, program efficiency, and production management to the dollar.

3D stacked die (Foveros) technology: Concept, HVM test strategy and associated DFT

Shridhar G Bendi, Sr. Principal Engineer (Intel)

Bio:

Shridhar Bendi has been with Intel-Bangalore Design for past ~19 years, mostly working on Xeon Servers. He currently serves as Sr. Principal Engineer, co-leading product design of SPR family of Servers catering to 5G vRAN. Prior to this, he served as DFx Arch. & Post-Si Design Debug Lead productizing 5+ Xeon family of Servers. Prior to joining Intel-India, he worked in US with AMD, TI, Cyrix and Intel. Shridhar has 15+ papers and multiple patents to his accreditation. He has Masters in Elect. & Computer Engg. and Materials Science & Engg. (Optoelectronics), Univ. of Florida, Gainesville

Abstract:
A quick overview of Intel's 3D stacked die (Foveros) technology and its play in heterogenous chip design world. While this technology provides upside on product goodness front, it poses unique challenges in high volume productization front. As part of this talk, will try providing sneak-peak into High Volume Manufacturing (HVM) challenges, strategy and associated DFT. Towards the end will touch upon potential areas of opportunity for EDA vendors.

TECHNICAL SESSIONS

Session 1 - Advancements in Design For Test

Session Chair | Dr. Ankush Srivastava

1.1 Enhancing At-Speed Testability of Complex Inter-Core IO Interfaces

Wilson Pradeep, Muniswara Vorugu and Vevekanenda Gonugunta

Abstract - With increased adoption of hierarchical DFT (Design for test) and core based test strategy, there is a great emphasis for effective at-speed testing of inter-core synchronous interfaces. Many design challenges exist which limit efficient usage of functional register reuse based core wrapping to enable it. To address this concern, we propose a novel customized core wrapper cell insertion methodology which allows seamless insertion of functional shared wrapper cells on non-supported sequential endpoints. Experimental results from applying the proposed method on a large hierarchical multi-core design indicate an improvement in shared wrapper cell usage in the range of ~6-8%, which aided in at-speed transition delay fault coverage increase by ~7.5 to 9% as compared to baseline approach. In cases where usage of shared wrapper cells is entirely infeasible, another alternative method is proposed which uses an overlapped scan configuration scheme to enable at-speed test of delay faults at core boundary. Application of combined test mode in another design showed a gain of 0 to ~92-95% delay fault test coverage improvement at the core boundary.

1.2 Selective Multiple Capture Test (SMART) XLBIST

Peter Wohl, John Waicukauski, Anushree Bhat, Vijay Kumar K S and Rajit Karmakar

Abstract—Logic BIST (LBIST) is increasingly deployed to realize test cost reduction and silicon life-cycle management. Xtolerant LBIST (XLBIST) expanded applicability to almost any design in the presence of unknown (X) values. XLBIST is crucial for many applications, particularly mission-critical applications such as aerospace/defense, automotive, telecommunications in- dustries etc. The optimization of test-time and test-cost are very important to reduce the overall latencies during In-System Test. In this paper, we introduce ATPG-driven multiple capture-clock selection which greatly increases XLBIST coverage per pattern. This helps in achieving the targeted coverage numbers with lesser number of seeds, greatly helping in test-cost reduction. Results with this novel solution on several big designs demonstrate consistent XLBIST coverage improvement even in presence of high X densities.

1.3 A novel fully automated multi-mode scan stitching architecture

Sarthak Singhal, Puneet Arora, Subhasish Mukherjee, Raghav Khemka and Krishna Chakravadhanula

Abstract - With more and more functionality being integrated into System-on-Chip (SoC) designs, the number of test mode configurations required to robustly test a given SoC are also increasing. Test mode configuration is a setup required to test SoC in a particular test methodology like production test, in-system test, stress test and so on. Every test mode configuration can have their unique scan constraints and requires creation of balanced scan chains. These constraints and requirements create a challenge for scan chain allocation, scan chain balancing in every test mode and automation. Existing solutions for these lead to non-scalable scripting, unwanted area overhead and long scan wirelengths due to addition of multimode multiplexers to take into account test mode crossings. This paper describes a new multimode scan stitching methodology which is highly customizable to serve ever growing Design-for-Test (DFT) constraints and scan connection requirements. This paper also introduces the innovative concept of scan groups to give user a simplistic yet powerful user-interface for multimode scan

stitching considering test clock domains, power domains, clock edges, scan chain balancing and multimode multiplexers optimizations.

Session 2 - 3DIC Test Challenges & Advanced Fault Models

Session Chair | Srinivasan Chandra Sekaran

2.1 TSV BIST Repair : Design-for-Test Challenges and Emerging Solution for 3D Stacked IC's
Akkapolu Sankararao, Vaishnavi G and Malige Sandya Rani

Abstract—The efficient methodology to increase the yield and performance of 3D Stacked Integrated-Circuits (3D SICs) using TSV BIST Repair mechanism is addressed in this paper. This technique provides a promising solution to overcome power and interconnect congestion issues encountered during TSVs pre-bond and post-bond tests of 3D stacked ICs. The proposed TSV BIST Repair approach has the ability to identify short, open, pin-hole, void and break defects in TSV bonding. In response to these defects, the repair mechanism will provide redundancy analysis and repairable features to defective TSVs. Finally, the complete analysis of the proposed TSV BIST repair methodology shows significant improvement of 14.5% yield and test cost by potentially recovering all eminent defective chips.

2.2 Accurate Diagnosis of Cell Internal Defects with Multiple Excitation and Propagation Conditions,
Sonam Kathpalia, Sameer Chillarige, Bharath Nandakumar, Madhur and Santosh Malagi

Abstract - Cell-aware fault models are created to model multiple classes of cell-internal defects such as cell-internal shorts and bridges. These cell-aware fault models significantly aid in improving the test quality and diagnosability of the failing Integrated Circuits (IC). Cell-aware faults models are typically created to minimize the number of faults modeled ensuring that all the cell-aware defects are covered with the minimal set of faults created. This is a good approach for ATPG but poses challenges for diagnosis accuracy and resolution. This paper talks about improving accuracy, and resolution of logic diagnostics, by proposing a novel technique to improve the results of logic diagnostics by combining simulation results of multiple cell aware faults to accurately identify the cell aware defect behavior and physical location. Experimental results on industrial design using thousands of failing samples indicated ~14% accuracy improvement with the proposed approach.

2.3 An Efficient Test Time Model for Optimizing Tessent SSN for a 3D Design
Vasubabu Ravipati, Shyam N Kallepalli and Lance C Cheney

Abstract—This paper presents an efficient scheme to calculate and optimize test time when using Tessent Streaming Scan Network (SSN) by bypassing the traditional vendor solution of patterns re-targeting process. SSN retargeting process requires stand-alone patterns of all partitions present in SSN network and availability of full chip SoC Netlist model which is too late in the design cycle. Many "case" studies can be performed for estimating test volume/test time, easily without hardware changes using the described algorithm in the paper. This methodology helps to update test network design for optimal test time and volume in very early phase of the project, thereby reducing iterative and late change costs for DFT design.

Session 3 - Optimizations in Silicon Manufacturing & Test Application

Session Chair | Srinivas Vooka

3.1 Transfer-Matrix Abstractions to Analyze the Effect of Manufacturing Variations in Silicon Photonic Circuits

Pratishtha Agnihotri, Priyank Kalla and Steve Blair

Abstract—The emergence of Silicon (Si) photonics necessitates the development of automated testing and validation techniques. Si-photonic device operation is sensitive to variations in the manufacturing process. This paper describes a methodology and abstraction models to evaluate the effect of variations in critical waveguide dimensions on Si-photonic circuits. Such variations may result in signal degradation and phase mismatch, causing interference based devices to operate imperfectly. Experiments are performed on various (linear) optical devices by introducing geometric and layout deformities, and compact models are abstracted in terms of Transfer Matrices. Using these models, we show how the impact of design or manufacturing variations in a device can be analyzed on the operation of optical logic circuits that integrate various such components. The method is validated by experiments performed on conventional SOI waveguide based devices and circuits.

3.2 Towards Complete State Machine Traversal via Pseudo Transitions in Automated Lab Verification

Marc Huppmann, Manuel Harrant, Thomas Nirmaier, Andi Buzo, Linus Maurer and Georg Pelz

Abstract—The complexity of modern automotive smart power devices increases due to their growing amount of functionality. The resulting extensive internal state machine requires more ver- ification time especially in the mixed-signal post-silicon domain, which still relies on manually intensive directed testing. A state transition based methodology is proposed, that automatically finds a verification path through the complete state machine and ensures that each transition, and hence each state, is traversed at least once. By extending the device´s state machine with pseudo transitions, that include information about the required lab setup configuration, a correct measurement of each requirement in question is ensured. Advanced graph theoretic algorithms can now be applied to cover all requirements that are associated to the state machine. In an industrial case study with an automotive smart motor controller it is shown that the methodology finds the optimal traversal through all 82 transitions of the device´s state machine. The automated adaption of the measurement setup, with regard to the load circuit and adequate measurement equipment selection, enables a correct verification of the requirements. This approach allows a lab-setup-agnostic automated formal verification of over 80% of the functional requirements and hence drastically reduces the time required for the formal mixed-signal post-silicon verification.

3.3 Implementation of Monotonicity Testing Utilizing On Chip Resources for Test Time Reduction

V Hemanthkumar

Abstract— Programmable System on Chip (PSoC) devices coming in to the market in recent times does possess basic elements such as configurable op-amps, counters, multiplexers,

onchip capacitors, switch matrix, Advanced High-performance Bus (AHB) etc. This paper presents an implementation to test monotonic parameters of SoC utilizing available hybrid bist options & thus reducing the overhead on Automated Testing Equipment (ATE) which has accounted for Test Time Reduction (TTR). This method has been verified on one of PSoC devices at both wafer (110 units) & package (3 units) level using MAGNUM1 NEXTEST ATE & found that test time has reduced by 28.31% compared to its traditional implementation of measuring voltage for each monotonic code.

Session 4 - Test Methodology, Validation and Power Aware Test

Session Chair | Bharath Nandakumar

4.1 Test Methodology Automation for Multi-Die Package Realization
Durga Prasad Bade, Rohini Gulve, Adam Cron and Mike Ricchetti

Abstract—Technological advancements in multi-die, chiplet, or other 3D architecture design are required to fulfill the high computational power needed for chips in the AI/meta world. Computing demands require die scaling, which can be achieved by fabrication of chips with chiplets integration in 3D. However, 3DICs designs requires new method and considerations for functional and test hardware access. This paper describes the hierarchical approach for DFT access of logic and memory dies through an IEEE 1838 compliant interface. This paper will introduce methodology to realize a stacked IC involving a) configuration and insertion of DFT at RTL, b) synthesis and fault list generation for TSV testing and other die-to-die connections, and c) test pattern porting for die-level test programs to the package pins.

4.2 Design of a programmable low power linear feedback shift register for BIST application
Maragathaeswari B and Geethu Remadevi

Abstract – In this paper, a programmable low power linear feedback shift register for BIST applications has implemented in Xilinx VivadoSuite 2019. The design is parameterizable for 'n-bit' polynomials and the seed value of user choice. Moreover, the design has a unique methodology of forcing low signal 0s in the dissimilar vector bits before the switching transition of registers and as well as incorporating the combination of two stage

LFSRs (DT-LFSR) which could successfully reduce the number of output vector transition by ~70% with respect to the conventional LFSRs and hence significant reduction in dynamic power due to switching activity between adjacent vectors. The design has synthesized and simulated for 4,8,16,32,and 64 bit LFSR of different polynomials

4.3 A System-Level Post-Silicon Validation Methodology for High-Speed Serial Interface
Sudeep Puligundla, Manikandan T, Paul Sunderland, Vineeth Vl, Anshu Gupta, Felix Tudoran, Christopher Daffron, Moises Puga Nathal, Tim Linn, Wayne Huang, Saikiran V, Sukay Luhadia and Scott Gardiner

Abstract—High-Speed Serial IO interfaces supporting data rates of several tens and hundreds of giga bits per second are ubiquitous in today's server and client platforms for chip-to- chip and board-to-board communications. Careful system level validation of these interfaces is critical for high quality product releases and is challenging in the constraints of tight validation cycles. This paper presents a post-silicon validation methodology applicable to such interfaces that is proven to be efficient in detecting bugs, both at the silicon and system level, enabling high-quality product releases on time.

Session 5 - Design for Security & Analog Test

Session Chair | Prof. Jayagowri

5.1 A Threshold based Hardware Trojan Detection Technique Using XGBoost Algorithm

Ranit Das, Tapobrata Dhar and Surajit Kumar Roy

Abstract—The globalization of Integrated Circuit (IC) manu- facturing has made ICs vulnerable to Hardware Trojans (HT). This paper proposes a gate-level netlist HT detection technique using Xgboost probabilistic classifier. Improved results are ob- tained using a threshold.

5.2 Performance Enhancement of Unsupervised Hardware Trojan Detection Algorithm using Clustering-based Local Outlier Factor Technique for Design Security

S Meenakshi and Nirmala Devi M

Abstract—Internet of Things (IoT) has become extremely prominent for industrial applications and stealthy modification deliberately done by insertion of Hardware Trojans has increased widely due to globalization of Integrated Circuit (IC) production. In the proposed work, Hardware Trojan is detected at the gate level by considering netlist of the desired circuits. To mitigate with golden model dependencies, proposed work is based on unsupervised detection of Hardware Trojans which automatically extracts useful features without providing clear desired outcomes. The relevant features from feature dataset are selected using eXtreme Gradient Boosting (XGBoost) algorithm. Average True Positive Rate (TPR) is improved about 30% by using Clustering-based local outlier factor (CBLOF) algorithm when compared to local outlier factor algorithm. The simulation is employed on Trust-HUB circuits and achieves an average of 99.83% True Negative Rate (TNR) and 99.72% accuracy which shows the efficiency of the detection method even without labelling data.

5.3 Functional Testing of On-chip Analog/RF Circuits using Machine Learning based Regression Model

Anshaj Shrivastava and Gaurab Banerjee

Abstract—This study aims to utilize the simulation data col- lected during the design stages of analog and RF Integrated Circuits (ICs), to enable faster functional testing during post- silicon validation. The above approach is demonstrated for an on- chip LC-Voltage Controlled Oscillator (LC-VCO) circuit, which was fabricated in a commercially available 180nm RF CMOS process, as a part of a radar-on-chip system. The key idea is to build a Machine Learning (ML) based regression model that learns various correlations between a few internal DC-node voltages (or currents) and performance-metrics of the LC-VCO circuit, using block-level simulation data. During post-silicon IC- testing, this ML-model is then used to predict the tuning-curve of the LC-VCO by measuring the same DC-node data. Finally, preliminary silicon-based measurement results show that the proposed approach holds much promise as the difference between the predicted tuning curves and measured curves is within 5%.

TEST REALITY CHECK (TRC) TRACK

Session Chair | Anurag Jain & Vishal Vadhavania

TRC 1 Enabling Hierarchical Assembly Build (MSIE) to improve turnaround time and performance for DFT pattern verification
Anuj Gupta, Sudhakar Kongala and Om Prakash Mishra

Abstract: Traditionally, lot of focus is being put on the creating an optimized set of patterns that help to reduce the overall test time and cost for testing the design during screening process.. With more and more logic being added to designs, designers are presented with a problem of test time optimization. At the same time, they must support multiple test and debug features like compressed and uncompressed ATPG, pattern masking, diagnosis, MBIST, repair, etc. All these requirements add various modes of operations to SoC design and are required to be verified and validated before it is sent out for manufacturing.

In this article we will try to bring focus on one such area that has a significant impact on the overall turnaround time for design verification i.e. compile and simulation performance and machine resources required for the same. We will present a simple and efficient methodology to help improve the overall turnaround time for verification of DFT test patterns which also helps to reduce the machine resources required for achieving the same. Unlike the conventional (monolithic) simulation methodology that is widely used in the industry where all the compilation, elaboration & simulation happens in the one go, this technique uses divide & conquer approach provided by the simulators like xcelium, etc.

TRC 2 Enhanced Diagnosis on Scan and Memory Failures for 22ULL Tech Node
Arul Karthick Kumar, Vivek Roopchand and Balaji Duthae Srinivasan

Abstract: Scan and Memory validation is one of the critical production screening tests to identify and screen structurally defective parts. High fail rate in scan and Memory testing will affect product yield drastically. Identifying root cause behind failures would be challenging tasks especially in new process tech node enablement. In this paper, we have discussed enhanced diag approach on 3 aspects 1. Memory Fail Debug and Yield Improvement, 2. scan chain debug in memory chain and 4. Low voltage scan chain debug in Retention type flops. It also explains on enhancement on methodologies used compared to existing approaches in voltage dependent and random fail scenarios. This paper explains not only about debug approach and also design fixes enabled for successive revisions to improve yield for 22nm Tech Node. This paper provides solution on yield improvement avoiding structural defects and also enables tech node towards production enablement for future SoCs.

TRC 3 Validation Strategies to Achieve Zero Silicon bugs in DFT Logic
V N Sivakumar Avvaru, Souvik Sarkar, Prakash Kumar and Ashutosh Anand

Abstract: Building robust pre-silicon test strategies and environment empowers engineers to catch bugs early in the project life cycle and eventually makes silicon bug free. This paper aims on five strategies. With these five strategies, we can achieve Day-One Silicon bring-up with Zero pattern re-generation and Zero Silicon bugs in DFT logic.

TRC 4 A Novel approach of improving test coverage using Z01X functional fault grading technique

Sreenivasa Rao Vuttaravilli, Leela Krishna Thota and Srinu Kona

Abstract: Automotive chips with ISO 26262 standard propose safety critical applications with high test coverage metrics along with its self-testing ability. With such stringent requirements on complex system on chips, coverage metrics that gets computed at every stage of the flow should be considered avidly. Initial fault coverage estimation can be evaluated at the RTL level with shift left strategy. Once we proceed with the traditional gate level coverage evaluation, there could be few cases where we may not be able to meet such rigorous coverage requirements. With functional faults, longer run times are observed where there is a lot of scope in improvising the computational speed by handling the fault dictionary effectively. In such cases, we depend on fault grading techniques. This paper defines a generic and structured approach that could be followed from scan fault coverage when combined with functional vectors to generate the incremental coverage using Z01X. This is demonstrated with the experimental data computed on various designs.

ACADEMIA RESEARCH TRACK

Dr. Ankush Srivastava, Qualcomm India Pvt Ltd,

Prof. Usha Mehta , Nirma University, Ahmedabad

The 6th Edition of International Test Conference, India, for the first time, will provide a unique platform for master's students, research scholars and post-docs to discuss novel research ideas, publication, funding advice and career opportunities from an established practitioner/Industrial liaison within their field. For the first time, ITC India is offering a "conference-sponsored Research Mentorship Program" to assist students in finding industrial liaisons and gain valuable insights on high-impact research ideas in the area of VLSI testing, Diagnosis and Reliability.

For the master student interested in VLSI Testing, this is the opportunity to network with industry liaisons to learn about test problems where industry is looking for solutions, and fine-tune the research objectives, based on the feedbacks.

For a research scholar/ Post-Doc interested in impacting industry with ideas? Apart from establishing collaborative relationships with industry liaisons, this is your opportunity to learn about, how their area of research fits within the industrial context. This engagement will also help them evaluating their ideas on industrial designs and protecting the technology by patenting the idea based on the main guide discretion.

How It Works?

Each selected candidate will be paired with at least two industrial liaisons. Over the course of the program, mentees will benefit from a series of about 8 one-on-one mentorship sessions taking place online, or in person.

All selected mentees will be required to attend an orientation session at the beginning of the program where they will be introduced to their liaisons. This session will also be an opportunity to learn about "best practices" in mentorship relationships, as well as other programs available through the academic research track (ART) platform, under the banner of ITC India.

This one-year mentoring relationship is intended for July 2022 to June 2023. will be extended based on the liaisons' s recommendation, along with main guide discretion.

Mentoring conversations should focus on research advice, professional advancement, publishing/funding strategies, and facilitating contacts.

Mentees should not offer or be requested to carry out work for the Industrial liaisons, and the engagement should be in line with the current research focus of the mentees.

If appropriate and by mutual agreement, Industry liaisons may also serve as official co-guide/Research-Advisory-Committee at the main guide discretion.

Industrial Liaisons may be invited for in-person activities at the academic institutes for additional discussions, lectures, tutorials, and future research activities that can be explored by any of the students of the respective departments.

POSTERS

Authors	Title
Vijay Kumar K S, Anushree Bhat and Jagdish Gudda	Novel X-tolerant LBIST with asynchronous clock support for optimized test-time
Balajiraja Ravinarayanan, Michael Morgan and Yean Fern Yeoh	Accelerating Array Fault Diagnosis using Validated Logical-to-Physical Mapping
Darshal Patel, Pradip Kapure, Praveen Ipe and Imtiaz Ahmed	Power efficient modular DFT architecture
Ananth G S, Mahadev G and Sanoop S	Power Integrity Simulations to aid ATE Hardware design for Reliability and Reusability
Vishwa Deepika Sripada, Jhansi Komala Nallapati and Satya Kumar Somisetty	At-speed Coverage Improvement for Complex AI SoC
Meghana Hampali and Jayagowri R	Implementation of secure scan architecture for scan based testing with area optimization
Viral Mehta and Kamya Ahuja	On Product Clock Generator- Todays necessity to At-speed testing
Priyanka Joshi, Sreenivasa Rao Vuttaravilli, Tushar Jeevan and Leela Krishna Thota	Convergent Glitch detection framework on complex Automotive Designs
Prashanth J V and Shivaranjani S	Whitespace reduction to minimize test time in hierarchical SoC designs
Dineshkumar C, Nirmala Devi M and Vaishnavi Sankar	Enhanced Reliability for VLSI Circuits through an Isolation Forest based Hardware Trojan Detection Method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