INDIA

IEEE International Test Conference, India 2019
July 21-23, The Leela Palace, Bengaluru

Tutorials @ ITC, India 2019

In addition to hosting a rich technical program, ITC India has been bringing together subject matter experts to deliver Tutorials on various topics of relevance. There are a total of six tutorials planned for the 3rd ITC India conference, covering a gamut of advanced topics spanning across pre-silicon and post-silicon aspects of test. These are meant to provide in depth understanding on the topics that they cover. They also provide the opportunity to interact with known experts from the industry and academia.

On the pre-silicon DFT techniques, there are tutorials on hierarchical test strategies, and DFT of AI chips. The former one will explain how using a divide-and-conquer approach, optimisations are possible on test implementation, pattern creation, test application, and diagnosis times. The latter tutorial will cover the architecture of the AI chips and how DFT is implemented on the real AI chips.

On post silicon test, there are topics on memory test and repair, defect based testing, post silicon validation and ATE load board design. The tutorial on memory test and repair will present the techniques needed for detection of defects during manufacturing and during life time, in today's FinFET devices. The presentation on defect based testing will cover the evolution of fault models and how ATPG can be used to detect these increasingly parametric faults.

Silicon debug continues to be a challenge for complex SoCs designed on new technology nodes. The tutorial on post silicon validation will focus on methods and examples of extending the validation continuum from pre-silicon to post-silicon, based on the work from the IEEE CEDA System Validation and Debug Technology Committee's Coverage Working Group.

Load-Board Design plays a vital role in deciding the overall testability features, test quality and cost of a product. Industry experts will present a tutorial covering the challenges and best practices in the ATE load board design.

As you can see, there is a variety of topics that will be covered during the Tutorial program at the 3rd ITC India Conference. We invite you to attend these sessions and benefit from the technical expertise and the multiple years of experience of the presenters. For more details on the **Agenda**, **Tutorial program** and **registration**, please visit the **ITC India web page.**

Venkat Totakura
Tutorial Chair

Jais Abraham
Vice Tutorial Chair