Sunday, July 21, 2019			
8:30am-9:30am	**REGISTRATIONS**		
TRACKS	**TRACK 1** Session Chair | Jais Abraham	**TRACK 2** Session Chair | Sivanantham	**TRACK 3** Session Chair | Venkata Rangam Totakura
HALL NAME	Grand Ball Room	Turret	Royal Ball Room
9:30 am - 11:00 am (15 mins. Break) 11:15 am - 12:45 pm	**T1: Memory Test and Repair in FinFET Era** Yervant Zorian (Synopsys)	**T2: Expanding the Validation Coverage continuance from Pre-Silicon to Post-Silicon** Nagabhushan (Intel), Gaurav Verma (NXP), Gupta Ashish (NXP)	**T3: AI Chip Technologies and Its DFT Methodologies** Yu Huang (Mentor), Rahul Singhal (Mentor), Lee Harrison (Mentor)
12:45pm-1:45pm	**LUNCH BREAK**		
1:45 pm - 3:15 pm (15 mins. Break) 3:30 pm - 5:00 pm	**T4: Creation and Selection of Fault Models for Defect Based Testing** Rubin Parekhji (TI), Wilson Pradeep(TI)	**T5: Challenges and Best Practices on ATE Load Board Design** Gowri Shankar (Tessolve), Jagadish (Tessolve), Srinivasan. C (Tessolve)	**T6: Practical Hierarchical Test Strategies for SoCs of Today and Tomorrow** Jay Jahangiri (Mentor), Nagesh Tamarapalli (AMD)