Monday, July 22, 2019		
8:00am-9:30am	REGISTRATIONS	
9:15am-9:40am	Inauguration/Welcome | Navin Bishnoi, General Chair, ITC India	
9:40am-9:45am	Special Talk on "ITC 50 Years" | Dr. Yervant Zorian, General Chair, ITC US	
9:45am-10:20am	Keynote 1: "Automotive electronics – the key driver of innovation in quality of test" | Dr. Janusz Rajski, Mentor, a Siemens Business	
10:20am-10:55am	Keynote 2: "Test – the wild west of advanced nodes Discontinuities coming in test development" | Michael Campbell, Qualcomm	
10:55am-11:15am	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 1 - Debug & Diagnosis Session Chair | Pramod Notiyath	Special Session 1 - Defect based Test Session Chair | Arvind Jain
HALL NAME	Grand Ball Room	Royal Ball Room
11:15am-12:45pm	**1.1 Improved Diagnosis Methodology for Multi-Defect Scenarios in High Compression Scan Based Designs** *Bharath Nandakumar, Sameer Chillarige, Anil Malik, Atul Chhabra, Wilson Pradeep and Prakash Narayanan* **1.2 High Throughput chain diagnosis methodology with minimal failure data collection** *Anil Malik, Atul Chhabra, Bharath Nandakumar, Sameer Chillarige and Kanika Kanwal* **Improving Diagnosis Resolution and Performance at High Compression Ratios (Invited paper)** *Sameer Chillarige, Atul Chhabra, Anil Malik, Bharath Nandakumar, Joe Swenton, Krishna Chakravadhanula*	**S1.1 Defect Location Identification for Cell-Aware Test** *Santosh S Malagi* **S1.2 Utilizing Delta IDDQ to Screen Cell Specific Defects for High Quality and Reliability Applications** *Ajay Rasquinha*
12:45pm-1:45pm	LUNCH BREAK	
HALL NAME	Grand Ball Room	
1:45pm-2:15pm	**Panel Discussion: Functional Safety Test Solution: Requirement or Marketing Buzz** **Panelist:** *Punit Kishore, Nilanjan Mukherjee, Adit Singh, Prasanth V, Amit Agarwal*	**Exhibit/Booth**
2:15pm-3:15pm		
3:15pm-3:30pm	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 2 - Test Cost Session Chair | Wilson Pradeep	Special Session 2 - mmWave Test Challenges Session Chair | Abhishek Chaudhary
HALL NAME	Grand Ball Room	Royal Ball Room
3:30pm-5:00pm	**2.1 Test cost reduction through increase in multi-site testing with reduced scan-out pins** *Jaidev Shenoy, Kushal Kamal, Kelly Ockunzzi and Virendra Singh* **2.2 Demonstration of On-Chip Test Decompression for EDT using Binary Encoded Neural Autoencoders** *Philemon Daniel, Shaily Singh, Garima Gill, Anshu Singh Gangwar, Bargaje Ganesh Pandurang and Kaushik Chakrabarti* **Advanced Techniques for Atspeed Exception Analysis (Invited paper)** *Omar Sharif Cherukur, Abhishek Bhattacharya, Piyush Ajmire, Gourav Biyani, Kamlesh Bhesaniya and Mahesh Rawal*	**S2.1 mmWave challenges in test** *Prof.Gaurab Banerjee* **S2.2 mmWave Test solution** *Sudhakar Babu*
5:30pm-6:30pm	Evening Cultural Program	
6:30pm-9:00pm	Banquet Keynote: "Moving Test to the Fast Lane: New paradigm leaves existing test throughput in the dust" | Steve Pateras, Synopsys NETWORKING DINNER	

Tuesday, July 23, 2019		
8:30am-9:30am	REGISTRATIONS	
9:30am-9:45am	Welcome / Day 1 Summary | Navin Bishnoi, General Chair, ITC India	
9:45am-10:20am	Keynote 3: "The Evolving Business Case for DFX" | Kaushik Narayanun, Nvidia	
10:20am-10:55am	Keynote 4: "IC Test – Where the Excitement Never Ends" | Rohit Kapur, Cadence	
10:55am-11:15am	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 3 - Silicon Validation Session Chair | Sathya K	Special Session 3 - Automotive Test Session Chair | Eswar Vadlamani
HALL NAME	Grand Ball Room	Royal Ball Room
11:15am-12:45pm	**3.1 Leveraging IEEE 1850 Property Specification Language and Mixed-Signal Assertions for Post-silicon Verification of Automotive Power Devices** *Thomas Nirmaier, Manuel Harrant, Bjoern Eversmann and Georg Pelz* **3.2 Applications of test techniques for improving Silicon to Pre-silicon timing correlation** *Reecha Jajodia, Kevin Zhou, Jaison Kurien, Tezaswi Raja, Manikandan P, Kartik Joshi, Prashant Singh, Vinayak Srinath, Jonathon Colburn and Sarvesh Sharma* **3.3 Debug for root causing SNR degradation due to dither in high performance pipeline ADC** *Himanshu Varshney, Viswanathan Nagarajan and Rajendrakumar Joish*	**S3.1 Automotive Test Challenges** *Prof. Adit Singh* **S3.2 Deterministic Stellar BIST for In-System Automotive Test** *Y. Liu, N. Mukherjee, J. Rajski, S.M. Reddy, J. Tyszer*
12:45pm-1:45pm	LUNCH BREAK	
SESSIONS	Special Session 4 - ITC ASIA Invited Papers Session Chair | Sameer Chillarige	Special Session - Academia Connect Session Chair | Vineet Srivastava
HALL NAME	Grand Ball Room	Royal Ball Room
1:45pm-3:15pm	**S4.1 An Empirical Approach to RTL Scan Path Design Focusing on Structural Interpretation in Logic Synthesis** *Tsuyoshi Iwagaki, Sho Yuasa, Hideyuki Ichihara and Tomoo Inoue* **S4.2 Optimization of Cell-Aware ATPG Results by Manipulating Library Cells' Defect Detection Matrices** *Zhan Gao, Erik Jan Marinissen, Min-Chun Hu, Joseph Swenton, Santosh Malagi, Jos Huisken and Kees Goossens* **S4.3 Accurate and Fast Time Testing Technique of Operational Amplifier DC Offset Voltage in µV-order by DC-AC Conversion** *Yuto Sasaki, Kosuke Machida, Riho Aoki, Shogo Katayama, Takayuki Nakatani, Jianlong Wang, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, Anna Kuwana, Kazumi Hatayama and Haruo Kobayashi*	**Academia Connect** **Moderator:** *Vineet Srivastava*
3:15pm-3:30pm	TEA/COFFEE BREAK SESSION	
SESSIONS	Session 4 - Beyond Chip Test Session Chair | Kavitha Shankar	Special Session 5 - Test Challenges Session Chair | Kamlesh Pandey
HALL NAME	Grand Ball Room	Royal Ball Room
3:30pm-5:00pm	**4.1 Hybrid emulation approach in ISO 26262 compliant unit test process** *Narendra Varma Alluri, Pradeep Reddy Sykam and Harish Narayanaswamy* **4.2 A hierarchical approach to self-test, fault-tolerance and routing security in a Network-on-Chip** *Ravikumar C.P., Kendaganna Swamy and Uma B.V.* **4.3 GPU-HBM SiP Interconnect Link Testing and Repair** *Amanulla Khan, Himakiran Kodihalli, Thenappan Nachiappan, Sreekar Sreesailam, Seth Chou and Colin Lee*	**S5.1 Test Challenges for Low Power SoCs** *Jais Abraham* **S5.2 Server DFT Challenges** *Nagesh Tamarapalli*
5:00pm-5:30pm	Closing Ceremony	