International Test Conference (INDIA) 2018 - Program Agenda

Tutorials

Sunday, July 22, 2018			
8:30am-9:30am	REGISTRATIONS		
TRACKS	TRACK 1	TRACK 2	TRACK 3
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B	ARABICA & ROBUSTA
9:30 am - 11:00 am (15 mins. Break) 11:15 am - 12:45 pm	**T1: Machine Learning in Test** Dr.Yu Huang, Gaurav Veda; (Mentor - A Siemens Business)	**T2: Automotive Reliability & Test Strategies** Dr. Yervant Zorian (Synopsys), Riccardo Mariani (Intel);	**T3: Test Access Mechanism (TAM) for Advanced SoCs** Punit Kishore, Jais Abraham (Qualcomm), & Shamitha Rao, Srijesh Parambath (Mentor - A Siemens Business)
12:45pm-1:45pm	LUNCH BREAK		
1:45 pm - 3:15 pm (15 mins. Break) 3:30 pm - 5:00 pm	**T4: Are System Level Tests Unavoidable for High End Processors?** Dr. Adit D. Singh, Auburn University	**T5: Recent Trends in Modelling and simulation of Defects in Analog Circuits and their Applications** Vijay Kumar Sankaran (Cadence), Lakshmanan Balasubramanian (Texas Instruments), Nadeem Tehsildar (Texas Instruments)	**T6: Logic Encryption: A Design-for-Security Trust Methodology for Digital Integrated Circuits** Prof. Santanu Chattopadhyay, Rajit Karmakar; IIT-Kharagpur

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Conference

Monday, July 23, 2018		
8:00am-9:30am	REGISTRATIONS	
9:30am-9:50am	Inauguration/Welcome | Navin Bishnoi, General Co-Chair, ITC India	
9:50am-10:20am	Keynote 1: "Infrastructure IP for Today's Automotive SOCs" | Dr. Yervant Zorian, Synopsys	
10:20am-10:50am	Keynote 2: "Testing in Always on Era" | P Raja Manickam, Tessolve	
10:50am-11:15am	TEA/COFFEE BREAK SESSION | SPONSORED BY CYIENT	
SESSIONS	SESSION 1 - MEMORY TEST & REPAIR Session Chair: Animesh Khare	SESSION 2 - DEBUG & DIAGNOSIS Session Chair : Arvind Jain
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
11:15am-12:45pm	**1-1. Improved RAM Sequential Tests for SoCs with Complex Memory Architectures** Wilson Pradeep and Prakash Narayanan **1-2. Automated Identification of Embedded Physical Memories using Shared Test Bus Access in IP Cores** Puneet Arora, Norman Card, Steven Gregor, Navneet Kaushik and Prashant Kulkarni. **1-3. Catalyst & Optimized Vector generation Methodologies for BIST and Multi-Core Repair Validation** Boopala Krishnan, Sumit Emekar, Prasanna Ramanujam and Subrahmanya M.	**2-1. High Accuracy, Robust Multiple Defect Diagnosis Scheme** Bharath Nandakumar, Anil Malik, Sameer Chillarige, Anshul Kumar, Joe Swenton and Atul Chhabra. **2-2. Pylon: Towards An Integrated Customizable Volume Diagnosis Infrastructure (Invited)** Atul Chittora, GLOBALFOUNDRIES **2-3. High Throughput Multiple Device Diagnosis System (Invited)** Sameer Chillarige, Anil Malik, Joe Swenton, Krishna Chakravadhanula
12:45pm-1:45pm	LUNCH BREAK	
1:45pm-2:15pm	Special Talk on "5G mm Wave Future Testing Methodology at ATE level", | ARABICA & ROBUSTA Tan Kheng How, Regional Application Consultant, Advantest	Exhibits / Booth
2:15pm-3:15pm	Demo Session by Advantest | Hall : ARABICA & ROBUSTA A Game Changer: Evolutionary system to highly efficient design evaluation	
3:15pm-3:30pm	TEA/COFFEE BREAK SESSION | SPONSORED BY CYIENT	
SESSIONS	SESSION 3 - AUTOMOTIVE TEST Session Chair | Kamlesh Pandey	SESSION 4 - MIXED SIGNAL & ANALOG TEST Session Chair | Rajesh Khurana
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
3:30pm-5:00pm	**3-1. Enhancing Automotive Self-Test with Embedded Distributed Programming** Carl Wisnesky II and Patrick Gallagher. **3-2. Breaking Test Coverage and Test Cost Barrier for Safety Critical Automotive Designs Targeting Zero DPPM** Wilson Pradeep, Aravinda Acharya and Nikita Naresh. **3-3. DFT strategy in automotive devices with low cost testing requirements** V Srinivasan, Sabyasachi Das, Manish Sharma and Tripti Gupta.	**4-1. Modeling and Simulation of Defects in Analog Circuits: Fault Modeling, Simulation and Coverage Calculation** Vijay Kumar, Lakshmanan Balasubramanian, Victor Zhuk and Nadeem Husain Tehsildar. **4-2. RF Senstivity test(7.5GHz) in non RF configuration using on board components** Sivapavan Anala, Purnachandra N, Jagadish Chandrasekaran and Srinivasan Chandrasekaran. **4-3. Challenges in analog loopback testing for RF transceivers** Nagarajan Viswanathan, Vidhya Lakshmi M, Nithin Gopinath, Shuhood Mohamed and Subbarao Nalluri.
5:30pm-6:30pm	Panel Discussion: "Fault tolerance or fault intolerance: what's the way forward?"	
6:30pm-9:00pm	NETWORKING DINNER	

International Test Conference (INDIA) 2018 - Program Agenda

Tuesday, July 24, 2018		
8:30am-9:30am	REGISTRATIONS	
9:30am-9:40am	Welcome / Day 1 Summary | Navin Bishnoi, General Co-Chair, ITC India	
9:40am-9:55am	Special Talk on "Test Technology Technical Council (TTTC)" |Dr. Yervant Zorian, TTTC Chair	
9:55am-10:25am	Keynote 3: "Self-Driving Cars – how they are pushing the boundaries of IC Testing." | Nilanjan Mukherjee, Mentor - A Siemens Business	
10:25am-10:55am	Keynote 4: "Directions in Advanced Packaging Technology" | Ravi Mahajan, Intel	
10:55am-11:15am	TEA/COFFEE BREAK SESSION | SPONSORED BY CYIENT	
SESSIONS	SESSION 5 - DFT ARCHITECTURE Session Chair | Pramod Notiyath	SESSION 6 - TEST CHALLENGES Session Chair | Hasan Sheikh
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
11:15am-12:45pm	**5-1. Testability of High-speed On-Chip Interconnect on ATE** Vishwajit Reddy, Amanulla Khan, Pradeep Bhat, Vinod Pagalone, Punj Pokharel and Suhas Satheesh. **5-2. A Novel Test Wrapper Architecture Design for Scan as well as Functional Test** Khushboo Agarwal and Ahmet Tokuz. **5-3. IP Design for Test Considerations for an Automotive End Application** Teresa McLaurin and Ke Peng.	**6-1. HBM operation and testing challenges** Narayanaswamy Muniyappa, Arun Kumar Chockalingam and Neelakandan Eswaran. **6-2. Test and Characterization of High Speed I/Os** Harsh Baghel, Vinod Kolluru and Krishna Rajan. **6-3. Test of Low Cost Microcontrollers: Challenges and Solutions (Invited)** Malav Shah, Texas Instruments
12:45pm-1:45pm	LUNCH BREAK	
1:45pm-2:45pm	**Demo Session by Advantest | Hall : Arabica & Robusta** A paradigm shift : CloudTesting™ Service for Skill development & Design	Exhibits / Booth
2:45pm-3:10pm	TEA/COFFEE BREAK SESSION | SPONSORED BY CYIENT	
SESSIONS	SESSION 7 - TEST POTPOURRI Session Chair | Kanwaldeep Sobti	SESSION 8 - STANDARDS Session Chair | Vikram Somaiya
HALL NAME	GRAND VICTORIA - A	GRAND VICTORIA - B
3:10pm-4:40pm	**7-1. Post Fabrication Fix for RF DIB Design Problems** Jagadish Chandrasekaran, Kandhan Rajakumar, Srinivasan Chandrasekaran and Gowrishankar Ilankumaran. **7-2. Hardware Trojan Prevention and Detection Used in Integrated Circuits** Jayanthi Daniel and Joshi Hrushikesh. **7-3. Power Efficient Circuit implementation for High Speed Digital Design** Renuka Nagapurkar.	**8-1. Practical aspects of a IEEE 1687 (Invited)** Rajesh Khurana, Cadence Design Systems; Sreekanth Pai, GLOBALFOUNDRIES **8-2. Meeting ISO 26262 requirements for analog and digital ICs (Invited)** Stephen Sunter, Mentor - A Siemens Business
5:00pm-5:30pm	Awards Function / Closing Ceremony	