



JULY 19–21, 2026



HOTEL RADISSON BLU,
BENGALURU

10TH IEEE

INTERNATIONAL TEST CONFERENCE INDIA 2026

CONFERENCE PROCEEDINGS

Reimagining Test in the Era of
Intelligent Silicon

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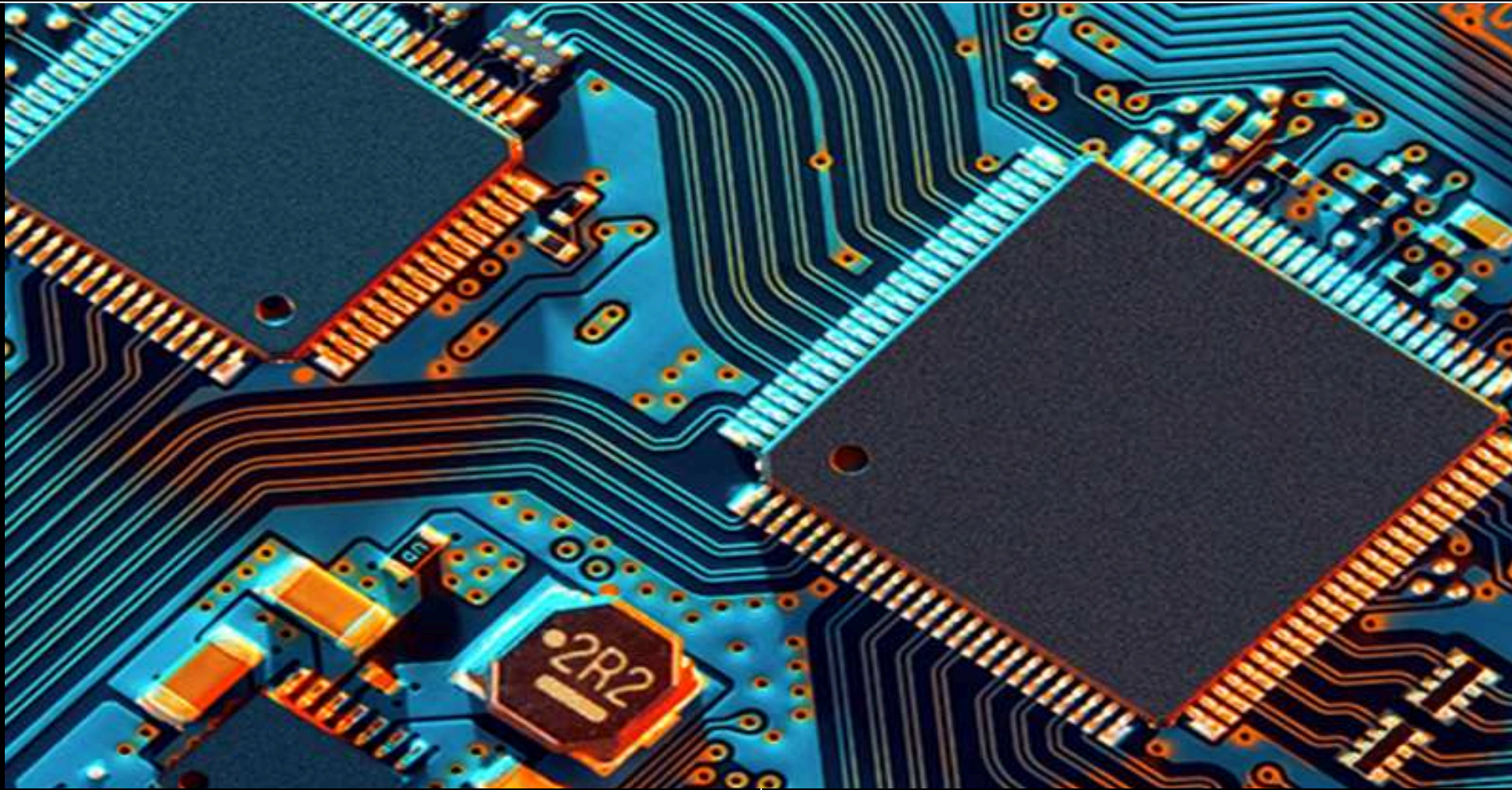
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MESSAGE FROM GENERAL CHAIRS



SIVANANTHAM S
VIT, Vellore



GAURAV BHARGAVA
Qualcomm, India

It is with immense pride and a deep sense of gratitude that we welcome you to the 10th edition of the IEEE International Test Conference India. What began a decade ago as a focused gathering of test and design-for-test professionals has grown into the country's premier forum for semiconductor test, reliability, and silicon lifecycle innovation — a milestone that reflects the remarkable maturing of India's semiconductor ecosystem. Reaching our tenth year in Bengaluru, at the very heart of the nation's silicon design activity, feels especially fitting at a moment when India is investing decisively in building an end-to-end semiconductor capability, from design and manufacturing to test, packaging, and assembly. This conference has always aspired to be more than a technical meeting; it is a place where academia, industry, EDA and equipment partners, and the next generation of engineers come together to shape the future of intelligent silicon.

This year's program embodies that ambition. Across keynotes, distinguished addresses, tutorials, technical tracks, industry sessions, panels, and a vibrant exhibit floor, you will find the full breadth of the field on display from DFT, chiplet and 3D-IC testing, and silicon debug to hardware security, reliability, and the accelerating role of AI in test. We are equally proud of the platforms that give our community its future, including the Academia Research Track, the Student Research Forum, and the hackathon, which continue to bring fresh talent and bold ideas into the fold. None of this would be possible without the dedication of our organizing committee, the generosity of our sponsors and exhibitors, the insight of our speakers, and above all, your participation. On behalf of the entire team, thank you for being part of this journey we hope you leave informed, inspired, and better connected.

MESSAGE FROM TECHNICAL PROGRAM CO-CHAIRS



SUBHADIP KUNDU

Cadence, India



ABHISHEK CHAUDHARY

AMD, India



NITHIN BHARADWAJ

Graphcore, UK

Welcome to the technical program of the 10th IEEE International Test Conference India. Assembling this program has been both a privilege and a responsibility, and we are delighted to present a slate of contributions that captures where semiconductor test stands today and where it is headed. This year's submissions reflect the growing complexity of modern silicon, heterogeneous integration, chiplet and 2.5D/3D architectures, advanced memory and high-speed interfaces, functional safety for automotive SoCs, and the rising importance of in-field reliability and silicon health monitoring. We are especially encouraged by the surge of work applying machine learning and AI across the test flow, from ATPG and diagnosis to yield analytics and post-silicon validation, alongside continued depth in DFT, IJTAG, hardware security, and ATE hardware design.

Every accepted paper reached these pages through a careful, peer-reviewed selection process, and we are grateful to the members of our Technical Program Committee and our reviewers, whose expertise and diligence upheld the technical quality this conference is known for. Our thanks also go to the authors who chose to share their work here including the students and early-career researchers whose contributions signal a bright future for the field in India and beyond, and to the track chairs and session organizers who gave the program its structure. We encourage you to engage generously: ask questions, challenge assumptions, and seek out the collaborations that so often begin in these rooms. We are confident you will find this program rich, relevant, and rewarding, and we look forward to the discussions it sparks.

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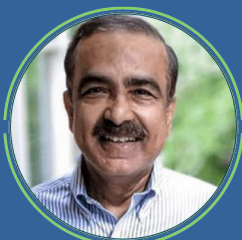


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Day 0 — Tutorials & Industry Test Challenge

Sunday, July 19, 2026

Time	Track 1 (Grand Victoria 1)	Track 2 (Grand Victoria 2)	Track 3 (Arabica & Robusta)	Track 4 (Brain Box)
08:00 AM–09:15 AM	Registrations			
	Session Chair: Bharath Nandakumar	Session Chair: Rajit Karmakar	Session Chair: Rama Sireesha Arisetti	Session Chair: Abhishek Chaudhary
09:15 AM–10:45 AM	Squeezing Quality into Cents: DFT Strategies for Low- cost MCUs Vishal Diwan and Mudasir Kawoosa (Texas Instruments)	LLM for VLSI Design, Automation and Test Chandan Karfa (IIT Guwahati)	Mission Mode Scan Dump Using IJTAG and TAP Customization: Architecture, Implementation, and Practical Considerations Sreekanth G Pai and Raseena KA (Marvell)	Testing Chiplet-Based 2.5D/3D ICs: An Academia/Industry perspective Binod Kumar, Manisha Kumari (IIT Jodhpur), Jaynarayan T Tudu (IIT Tirupati), Jyotirmoy Saikia and Sagar Kumar (Cadence)
10:45 AM – 11:15 AM	Tea/Coffee Break			
11:15 AM – 12:45 PM	Closed Loop Test Engineering – From Design to Mass Production Maheedhar J alasutram, Jeren Ku and Daejin Shin (Google)	Machine Learning is Inevitable or Not: A DFT Designer's View Ankush Srivastava (Qualcomm)	Beyond Scan Dump: Why IEEE P2929 Enables True Scan State Extraction Lee Harrison, Andy Hughes and Peter Orlando (Siemens EDA)	Testing Chiplet-Based 2.5D/3D ICs: An Academia/Industry perspective (<i>continued</i>) Binod Kumar, Manisha Kumari (IIT Jodhpur), Jaynarayan T Tudu (IIT Tirupati), Jyotirmoy Saikia and Sagar Kumar (Cadence)
12:45 PM – 01:45 PM	Lunch Break			
	Session Chair: Bharath Nandakumar	Session Chair: Rajit Karmakar	Session Chair: Rama Sireesha Arisetti	
01:45 PM – 03:15 PM	Testing to Self Testing: SelfTest Driven Functional Safety for ISO26262 Compliant AutomotiveSoCs Rajesh KumarTiwari and Mohammed Zuber P Malek (Qualcomm)	The Seamless Integration of Packetized Scan and In-system Test with Advanced ATE Equipment Lee Harrison (Siemens EDA) and Hagen Goller (Advantest)	Advanced Test Data Analytics for Yield and Quality Improvement Navya Rastogi, Shamitha Rao, Shrestha Hota (Synopsys) and Soumya Mittal (Qualcomm)	Industry Test Challenge (Invite Only) Talk1 Talk2 Break Talk3
03:15 PM – 03:45 PM	Tea/Coffee Break			Talk4 Break
03:45 PM – 05:15 PM	Understanding Test Escapes and the Limitations of Sean DFT Testing Adit Singh (Auburn University)	Scalable ATE Hardware Design: From Concept to Manufacturing with Reusable Architecture Lokapriya B, Senthilkumar Dhamodharan and Vaishnavi Saravanan (Caliber Interconnects)	Customer Centric Post Silicon Validation Approach for System on Chip (SoC) Ravishankar Manishankar and Siloni Pilani (Intel)	Panel: Correlation Crisis in Semiconductor Test: Can AI Bridge the Gap? Moderator: Sameer Chillarige (Cadence) Panelists: Udayakiran Yallamaraju (Qualcomm), John Schulze (AMD), C Jagadish Kumar (Intel), Raghu G G (Infineon)

06:30 PM – 07:45 PM			TTTC Workshop	
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Day 1 | Monday | July 20, 2026

Time	Track 1 (Grand Victoria 1)	Track 2 (Grand Victoria 2)	Track 3 (Arabica & Robusta)	Track 4 (Brain Box)
08:00 – 09:00 AM	Registrations			
09:00 – 09:30 AM	Conference Inauguration General Co-Chair, ITC India 2026 (Opening Remarks, Conference Highlights, Lamp Lighting by Chief Guests)			
09:30 – 11:00 AM	Keynote Addresses Designing Chiplets and 3DIC for Quality and Reliability - Yervant Zorian (Synopsys) Silent Data Corruption by 10x Test Escapes Threatens Reliable computing - Subhashish Mitra (Stanford University) SI Complexity to AI Revolution: India’s Silicon Leap 2047 - Senthilkumar Dhamodharan (Caliber Interconnect)			
11:00 – 11:05 AM	Exhibit Zone Inauguration			
11:05 – 11:30 AM	Tea/Coffee Break			
HALL NAME	GRAND VICTORIA 1	GRAND VICTORIA 2	ARABICA & ROBUSTA	BRAIN BOX
SESSIONS	Technical Track 1: 3D IC and Chiplet Testing Session Chair: Ashwini Shankar	Technical Track 2: Hardware Security and Trojan Detection Session Chair: Rajit Karmakar	Technical Track 3: Pre-Silicon Verification and Debug Session Chair: Manivannan Ethiraj	Special Session

11:30 AM – 12:45 PM				
	1.1: RL-Driven 3D Clustering of JScan Architecture with Routing and Area Optimization in Chiplet SiP Hilay Patel, Naman Kalra and Jaynarayan T Tudu (IIT Tirupati) 1.2: A Methodology for Robust Testing of Through Glass Vias (TGV) on Glass Substrate-based 3D Chiplets Manisha Kumari (IIT Jodhpur), Jaynarayan T Tudu (IIT Tirupati) and Binod Kumar (IIT Jodhpur) 1.3: Cost Aware Sector Symmetry and Wafer Cutting Methods for 3D ICs with Heterogeneous Defects Tanusree Kaibartta, Saksham Jha, Digvijay Anand Anand (IITISM Dhanbad) and Debesh Das (Jadavpur University) Best paper nominations	2.1: Innovative Memory Interconnect Architecture: Setting New Standards for Security, Safety and Performance in Real-Time Control MCUs Prasanth Viswanathan Pillai, Varshashree Kottadamane, Saya Goud Langadi, Labeeb K, Naveen Kothuri, Narendra Ravilla, Ramakrishna Pidaparthi, Rohit Chaudhari and Sivareddy Maramreddy (Texas Instruments India) 2.2: Test Pattern-Driven Detection of Hardware Trojans Using Switching Activity Analysis in FPGA-Based Systems Kannan S J, Chinakaku Lakshmi Prasanna and Sobhit Saxena (Lovely Professional University) 2.3: STAMP: Statistical Trojan Attribution via Multi-class Power-trace analysis Senthilkumar Dhamodharan, Sinthanai Selvi G, Karthika R and Abirami Vinayagamoorthy (Caliber Interconnects)	3.1: Comprehensive Coverage Framework for LPDDR6 Feature Validation: Navigating Complex Modes and Reducing the Verification Closure Gap Dharini Subashchandran, Gruhesh Patel, Meghna Ahuja and Shyam Sharma (Cadence Design Systems India) 3.2: A Novel Verification Method for Debug Tracing-in Close Chassis System Maneesh Pandey and Madhav Lekkala (Intel Technology) 3.3: Assertion Based Formal Verification of AES 128 Crypto Core Shivang Sharma (DRDO, SAG), Vineeth Jaisal (IIT Jodhpur) and Prashant Singh (DRDO, SAG)	Industry Showcase - 1 (11:30 AM- 1:00 PM): Evolving DFT Validation Methodologies for Complex Digital Designs Adir Zonta (Advantest) SSN and iJTAG aware ATE Hagen Goller (Advantest)
12:45 – 01:45 PM	Lunch Break			
SESSIONS	Technical Track 4: Advances in DFT and ATPG Session Chair: Nikila Krishnamoorthy	Technical Track 5: AI and Machine Learning Applications Session Chair: Mudasir Kawoosa	Technical Track 6: Secure IJTAG and Access Control Session Chair: Srijesh Parambath	Special Session
01:45 – 03:30 PM	4.1: Physically Aware Weighted Fault Model : A new paradigm in testing Sandipan Sharma, Srinivas Vooka, Maheedhar Jalasutram, Pranav Murthy (Google India Pvt. Ltd), Chieh-Jen Ku and Yanhan Zhu (Google LLC) 4.2: Rethinking RTL DFT: A Discrete RTL Flow for Parallel DFT Integration Mohan Raj Gopal, Veejaye Panayadian and Kundan Jha (SanDisk India Pvt Ltd) 4.3: A Novel Power-aware ATPG with Biaxial Transition Control for Extreme Low Power Targets Hanumant Tuntoni (Synopsys), Hillol Maity (Nvidia), Sreenu Kakanuri, Peter Wohl, Parthajit Bhattacharya, Bruce Xue and Geguang Miao (Synopsys) 4.4: Differential Evolution with Fitness-and Position-Based Selection in Search of Best Test Pattern for Combinational ATPG Manish Kumar, Isha Dubey, Priyajit Bhattacharya and Rahul Bhattacharya (IIT(ISM) Dhanbad)	5.1: Signal Integrity Simulation Hour Optimization: A Novel AI Framework Using Minute-Scale SI Predictor in High-Speed Test Interface Hardware Design Senthilkumar Dhamodharan, Lokapriya B, Dyaneswaran A, Karthika R and Lokendran S (Caliber Interconnects) 5.2: Post-Silicon Validation of Neuromorphic SoCs: A Hybrid BIST and ML-Based Approach for NVM Synaptic Fault Detection Kalyana Sundaram Chandran, Senthilkumar Dhamodharan and Sindhu Mathy S (Caliber Interconnects)	6.1: State-Isolated Scan - A Secure Low-Power Scan Architecture C.P. Ravikumar (Vinyana Tech) and Kushal C. (Sykatiya Technologies) 6.2: eFPGA-Enabled Dynamic Access Control for Secure IEEE 1687 (IJTAG) Networks Anekaït Thampi, Anshul Raghavendra Katti, Manish Nagaraju and Sudeendra Kumar K (PES University) 6.3: Design of a SAT-Resilient IJTAG Architecture for Secure and Scalable On-Chip Instrument Access Saravanan P, Dharani Sree K, Jothika K, Nivashini S and Sivaprabha Sri Pl (PSG College of Technology) 6.4: PQC-Based Secure Access Manager for IJTAG Network (ART Paper) Prajwal G S Basavaraj, Abhinav S, Arun Kumar N, Sudeendra Kumar (PES University, Bangalore)	Industry Showcase 2 - Teradyne (2:00 - 2:45 PM) Wafer to Rack. Chip to Cloud. Tested by Teradyne (Paresh Bharkhada, Teradyne) Industry Showcase 3 - Caliber Interconnects (2:45 - 3:30 PM)

01:45 – 03:30 PM	5.3: T-MAP: A Cross-Platform AI driven Test-Program Metadata Analysis Tool for Digital Coverage, Force, limit and Range Verification Kaushik Chakravorty, Dundapa Sankapal, Vishal Rohilla, Sudhish Raj Gj, Pratyush Dargan and Robert Cook (Texas Instruments) 5.4: AI-Driven IP Configuration Optimization for Post-Silicon Validation Akhilesh Tiwary, Maneesh Kumar Pandey, Nihar Chaniyara (Intel Technology India Pvt Ltd) and Utsav Banerjee (IISC Bangalore)	
03:30 – 04:00 PM	Tea/Coffee Break	Poster Session (ENTRANCE LOBBY)
HALL NAME	GRAND VICTORIA	
04:00 – 05:15 PM	Distinguished Addresses The critical role of Test Strategy in India's Semiconductor Growth - Alpa Sood (Teradyne) From Point Tools to Agentic AI: How EDA has impacted Semiconductor Industry - Don Chan (Cadence) The Intelligent Silicon Era: Redefining Semiconductor Test Through Innovation, AI, and Collaboration - Rajesh Vaddempudi (Advantest)	
05:15 – 05:30 PM	Closing Remarks General Co-Chairs, ITC India 2026	
05:30 – 06:30 PM	BREAK (NO ACTIVITY PLANNED)	
06:30 - 08:30 PM	Banquet Sit Down Dinner (Invite Only) ITC India - 10th Edition Reflections Panel: The Economics of Test: Where Should We Spend the Budget? Moderator: Navin Bishnoi, Marvell Panelists: Alpa Sood (Teradyne), Ruchir Dixit (Siemens), Gowrisankar A. (Caliber Interconnects), Jeff Rearick (AMD) Felicitation of the Past Committee Members Dinner	

Day 2 | TUESDAY | July 21, 2026

08:30 – 09:00 AM	Registrations			
HALL NAME	GRAND VICTORIA 1 & 2			
09:00 – 09:30 AM	Welcome / Day 1 Summary General Co-Chair, ITC India 2026			
09:30 - 11:00 AM	Keynote Addresses			
	AI in Test: Fear it or harness it - Jeff Rearick (AMD)			
	Built-in Intelligence - Leveraging Advanced DFT for Silicon Health monitoring - Nilanjan Mukherjee (Siemens)			
	From Silent Patient to Self-Healing Silicon: The Four Evolutionary Stages of DFT in Mass Production - Bizhan Delgoshaei (Google)			
11:00 – 11:30 AM	Tea/Coffee Break			
HALL NAME	GRAND VICTORIA 1	GRAND VICTORIA 2	ARABICA & ROBUSTA	BRAIN BOX
SESSIONS	Industry Session 1	Technical Track 7: ATE and Hardware Test Methods Session Chair: Veejaye Panayadian	Technical Track 8: Silicon Reliability and Lifecycle Management Session Chair: Sreekanth G Pai	ART Track 1
11:30 AM – 12:45 PM	Talk 1:A day in the life of a DFT Engineer – Can AI Agents help?, Jayashree Saxena, Vice President – Semiconductor DFT, Anora Labs Talk 2: Built-in Intelligence in Analog-to-Digital Converters, Nithin Gopinath, Senior Member Technical Staff, Texas Instruments Talk 3: System Level Test at Hyperscale : Transforming DFT for Data Infrastructure Nikhil Sudhakaran, Director of Engineering, Marvell	7.1: Real-Time Path Resistance Compensation and Spatial Diagnostics for High-Volume Wafer Test Sujith Thomas, Siva Elango S, Dinesh Sharma and Mathangi Raghuraman (SanDisk India Device Design Center Private Limited) 7.2: Polynomial Regression Based Qualitative Assessment of Automated Test Equipment Calibration Anand Venkatachalam (University of Stuttgart), Ernst Aderholz (Infineon Technologies AG,Munich), Matthias Sauer, Simon Schweizer, Matthias Werner (Advantest Europe GmbH) and Ilia Polian (University of Stuttgart) 7.3: A Novel Plug-In Module Architecture for Extending Automatic Test Equipment Capability to Wireless Testing of Pin-Less Semiconductor Devices Sathiyapriya Krishnamoorthy, Manoj Pachaiyan and Senthilkumar Dhamodharan (Caliber Interconnects)	8.1: Unified Compact Health and Aging Models for Manufacturing to In-Field Silicon Quality and Reliability Management Dan Alexandrescu, Shubharthi Datta and Leela Krishna Thota (Synopsys) 8.2: Reliability Refining Next Generation UV Cured Conformal Coatings under Harsh Environment Testing Aurkie Ray, Cole Sandvold, Andi Duffy, Bethany Turner, Saskia Hogan, Phil Kinner, Christopher Allen and Anna Lifton (Macdermid Alpha Electronics Solutions) 8.3: Design and Context Aware Embedded Monitor Analytics Through High-Volume Algorithmics and Explainable AI Dan Alexandrescu, Shubharthi Datta and Leela Krishna Thota (Synopsys)	ART1. A Unified Fault Detection and Repair Framework for Memristor-Based Non-Volatile Memories Aryan Anand and Vishal Gupta (VIT) ART2: Towards Secure IoT: A Lightweight PUF-Based Proximity-Aware Authentication Protocol for Resource-Constrained IoT Devices, Abdulla Syed, Navya Sri Tulluru and Mounika Mellamarthi (SRM University) ART3: Functional Safety Testing of On-Chip Cache Memories, Siyana Bijju, Simi Sukamaran and Tripti S Warriar (Cochin University of Science and Technology)

11:30 AM – 12:45 PM				ART4: Assertion-Centric UVM Verification of a Fault-Injectable 32-bit RISC-V ALU–IFU Subsystem, Divyanshi Sharma and Sandeep Patel (MANIT Bhopal)
12:45 – 01:45 PM	Lunch Break			
SESSIONS	Industry Session 2	Technical Track 9: Memory Test and MBIST Methodologies Session Chair: Ankit Garg	Technical Track 10: Post-Silicon Validation, Silicon Fixes, and Low-Power DFT Session Chair: Sreenu Kakunuri	ART Track 2
01:45 PM – 03:30 PM	Panel: India's Semiconductor Test Ecosystem: Growth story and Sustainability challenges. Moderator: Gaurav Bhargava (Qualcomm) Panelists: Jayashree Saxena (Anora Labs), Jaynarayan T. Tudu (IIT Tirupati), Dr. Rubin Parekji (Texas Instruments), Musunuri Surya (Infineon) Talk 4: Gopikrishna Siddula (SanDisk) : Testing High-Speed NAND Flash Interface I/Os for Silicon Quality and Production Readiness Talk 5: Anand Muthaiah (Tessolve) : On-chip Intelligence Transforming IC Testing.	9.1: Physical Design Aware Verification Methodology for Closing Coverage Gaps in SharedBus MBIST Shivam Tulsyan, Mayank Parasrampuria, Prachi Sinha, Vasudevan Pillai A and Maheedhar Jalasutram (Google India) 9.2: Constraint-Based Functional Testing of Encrypted Memory Systems *** Ravikumar C.P. (Vinyana Tech) 9.3: Enabling EDA Automation for HBM Testing Using A Plug-n-Play DFT Interface Quoc Phan, Anshuman Chandra (Siemens EDA), Bartosz Zelek (Poznań University of Technology), Barbara Działowska, Marta Stepniewska and Jonathan Gaudet (Siemens EDA) 9.4: Enhancements in Memory Test for improved diagnosability and comprehensive multi-bank test Prachi Sinha, Veerabhadrarao Vasa, Shivam Tulsyan and Mayank Parasrampuria (Google LLC)	10.1: A novel hardware design for effective supply voltage glitch injection Antony Varghese, Ashok Kumar and Asmita Mohapatra (Infineon Technologies India Pvt. Ltd.) 10.2: Validation Methodology to Characterize Absolute Propagation Delay, Delay variation over temperature and Programmable Delay of 1ps DNL step in Wideband RF Buffers up to 12.8GHz Harish Ramesh, Jason Xavier and Pranav Kumar (Texas Instruments) 10.3: DFT-Enhanced Spare Cell Architecture for Scan-Integrated ECO and Leakage Optimization in SoCs Pramod Gayakwad, Raghavendra H D, Chandhramohan K P, Khushboo Rathore, Vishwanath Kunchigi, Vamsi Krishna Oliveti and Santhosh Kamatam (NXP) 10.4: Hybrid Power Gating: Hardware Trio Framework based ATPG for Low-Power Scan (TRC Paper) Darshan V, Karthikeyan Soundararajan, Vivek Roopchand, Arul Karthick Kumar and Praveen Raghuraman (Qualcomm India Private Limited)	Hackathon Opening Remarks Team 1: A Fault Model for Guided-Wave Optical Interconnects in Die-to-Die Architectures Sanjay S. Subramaniam, Shaun Sebastian, Nishanth M., Gouri S. Nair (Indian Institute of Information Technology Kottayam, India) Team 2: Cross-Layer Degradation-Aware Fault Modeling and Adaptive Test Generation for FeFET Non-Volatile Memories Aashish Nirranjan Barathykannan, Akhilesh M., Shanganidhi K. N., Dinesh Babu A. (SRM Institute of Science and Technology, Vadapalani Campus, India) Team 3: Functional Fault Modeling for MAC-Based CNN Accelerators M R Harsha, Vanshika Kavi and Suresh G Kini (KLE Technological University)

01:45 PM – 03:30 PM				Team 4: Fault Primitive Taxonomy and MARCH-ReRAM: A Comprehensive Test Framework for Resistive RAM Arrays Addressing Manufacturing Defects and In Field Reliability Degradation Gautham P and Maithreyan S (Indian Institute of Information Technology Kottayam, India) Team 5: Observability-Based Functional Fault Modeling for RISC-V Processors Alan Paul, Niranjan K S, Kevin Jose and Adithya R Prabhu (Indian Institute of Information Technology Kottayam, India)
	Tea/Coffee Break			
	HALL NAME	GRAND VICTORIA 1 & 2		
	04:00 – 04:25 PM	Distinguished Address Semiconductor Test : A Product Perspective - Arojit Roychowdhury (Qualcomm)		
	04:25 – 05:30 PM	Panel: Scaling DFT in the era of AI, HPCs, Chiplets - Are traditional DFT approaches efficient for MCMs and Chiplets? Moderator: Kamlesh Pandey (Krivya Semicon) Panelists: Dr. Yervant Zorian (Synopsys), Dr. Shalini Pathak (STMicroelectronics), Rajesh Vaddempudi (Advantest), Srinivas Vooka (Google)		
05:30– 06:00 PM	Closing Ceremony Awards and Valedictory Session General Co-Chair, ITC India 2026			



Vishal Diwan, Texas Instruments

Vishal Diwan is a Digital Design Manager and Member Group Technical Staff at Texas Instruments, where he leads the DFT team for the ASM Business Unit. With over 13 years of experience in Design-for-Test methodologies, he has developed deep expertise across scan architectures, test automation, and advanced DFT implementation strategies for semiconductor products. He holds a Master's degree in Electrical Engineering from IIT Bombay and has contributed extensively to the field through multiple patents, technical publications, and presentations at industry conferences. His experience in developing efficient DFT solutions for cost-sensitive, high-volume semiconductor products has given him valuable insight into the trade-offs between test quality, silicon area, test time, and manufacturing cost. This practical perspective enables him to provide a comprehensive view of how innovative DFT methodologies can help deliver reliable MCUs while meeting the aggressive cost targets demanded by today's semiconductor industry.



Mudasir Kawoosa, Texas Instruments

Mudasir Kawoosa is a DFT Architect at Texas Instruments (India) Pvt. Ltd. in Bangalore, with fifteen years of industry experience. As a Senior Member of Technical Staff, he leads the centralized DFT team in Connectivity Business Unit driving transformative changes through innovative test solutions, expert silicon bring-up and widely adopted methodologies. Mudasir has architected DFT and test solutions for over fifteen complex System-on-Chip (SoC) programs. He holds master's degree in electrical engineering from the Indian Institute of Technology, Madras, has published in several peer reviewed external conferences (and is also prolific in TI internal and other conferences), and holds eleven granted US patents. Through his work, he has established several innovative solutions in DFT, test and silicon debug, for a wide variety of chip architectures across several business units in TI, and continues to influence the EDA DFT roadmap.

Squeezing Quality into Cents: DFT Strategies for Low-Cost MCUs

Abstract

Low-cost microcontrollers form the backbone of today's connected world, powering applications across IoT, automotive, industrial, and consumer markets. However, delivering high-quality, reliable MCUs at massive production volumes requires balancing stringent cost targets with demanding quality and safety requirements. This tutorial explores Design- for-Test strategies specifically tailored for cost-sensitive MCU designs, addressing challenges such as minimizing silicon overhead, reducing test time, optimizing ATE utilization, managing test power, and maximizing manufacturing throughput. Through practical examples and real-world methodologies, attendees will gain valuable insights into achieving high test coverage and low DPPM while operating within the tight area, power, and cost constraints that define modern MCU development

LLM for VLSI Design, Automation and Test

Dr. Chandan Karfa, IIT Guwahati

Abstract

The growing complexity of modern semiconductor systems is placing unprecedented demands on design, verification, and test workflows. As chips scale to billions of transistors and increasingly heterogeneous architectures, traditional EDA methodologies require significant manual effort and domain expertise to meet aggressive performance, power, and time- to-market targets. This tutorial explores how Large Language Models (LLMs) are emerging as powerful assistants for VLSI engineers, enabling higher levels of automation across RTL design, verification, synthesis, debugging, and test generation. Rather than replacing conventional EDA flows, the session examines how LLMs can augment engineering productivity, streamline development cycles, and redefine the way designers, verification engineers, and test professionals interact with semiconductor design tools in the AI era.



Dr. Chandan Karfa, IIT Guwahati

Dr. Chandan Karfa is an Associate Professor in the Department of Computer Science and Engineering at IIT Guwahati, where his research spans electronic design automation, formal verification, hardware security, high-level synthesis, and formal methods. Prior to joining academia, he spent five years as a Senior R&D Engineer at Synopsys, gaining valuable industry experience in semiconductor design automation. A prolific researcher, he has authored more than eighty publications in leading international journals and conferences and has been recognized with several prestigious honors, including the Google India Research Award, Google Silicon Research Awards, Qualcomm Faculty Award, and multiple innovation and best paper awards.

Mission Mode Scan Dump Using IJTAG and TAP Customization: Architecture, Implementation, and Practical Considerations



Sreekanth G Pai
Marvell

Sreekanth G Pai is a Senior Principal Engineer with extensive experience in Design-for-Test, scan architectures, IJTAG infrastructures, and post-silicon debug methodologies for complex SoCs. Throughout his career, he has led and contributed to multiple large-scale silicon programs, developing expertise in TAP customization, mission-mode debug techniques, and Tessent-based DFT implementations.



Raseena K A
Marvell

Raseena K A is a Senior Engineer specializing in DFT implementation, scan architectures, and post-silicon debug for complex SoCs. Her experience includes the development of IJTAG-based infrastructures, scan dump enablement, clock and OCC interactions, and customized debug solutions tailored to mission-mode applications. Through her work on silicon bring-up and debug using advanced scan and test methodologies, she has developed strong expertise in practical debug execution and validation workflows.

Abstract

As modern SoCs continue to grow in scale and complexity, effective post-silicon debug has become a critical challenge for ensuring rapid issue resolution and successful product deployment. Traditional test infrastructures often lack the observability required during mission-mode operation, creating the need for more flexible and scalable debug methodologies. This tutorial explores the use of IEEE 1687 (IJTAG) and TAP customization to enable mission-mode scan dump capabilities, providing efficient access to internal silicon states with minimal design impact. Attendees will gain insights into IJTAG-based architectures, scan data extraction techniques, implementation challenges, verification strategies, and practical considerations for enhancing observability and debuggability in advanced semiconductor designs.



Jyotirmoy Saikia
Cadence



Sagar Kumar
Cadence



Dr. Binod Kumar
IIT Jodhpur



Dr. Jaynarayan T. Tudu
IIT Tirupati



Manisha Kumari
IIT Jodhpur

Testing Chiplet-Based 2.5D/3D ICs : An Academia/Industry perspective

Abstract

The semiconductor industry is rapidly transitioning from monolithic System-on-Chip (SoC) designs to 2.5D and 3D multi-die architectures to meet the growing demands for higher performance, improved power efficiency, greater scalability, and faster time-to-market. While these advanced integration technologies offer significant system-level advantages, they also introduce unprecedented test and reliability challenges arising from heterogeneous integration, limited access to buried dies, complex die-to-die interconnects, and compounded yield loss across multiple stacked components. This tutorial provides a comprehensive overview of the testing methodologies for 2.5D and 3D integrated systems, covering the complete test flow from pre-bond and mid-bond testing to post-bond and system-level validation. Participants will learn about scalable Design-for-Test (DfT) architectures and standardized test access mechanisms that enable efficient delivery of test data through stacked dies while ensuring thorough validation of both individual dies and high-density die-to-die interconnects. Further, the tutorial also presents emerging AI-assisted testing methodologies for three-dimensional chiplet integration using micro-bump interconnects, where interface densities can reach thousands of connections per die. AI-based approaches for different types of interconnect defect detection and fault localization will be introduced, demonstrating how machine learning can significantly improve test quality and diagnostic accuracy for complex multi-die systems. Finally, the tutorial explores one of the latest advances in advanced packaging—glass substrate-based 2.5D/3D chiplet System-in-Package (SiP) technology. It discusses the unique testing challenges associated with Through Glass Vias (TGVs) and presents effective test strategies for ensuring the reliability and manufacturability of next-generation glass-based packages. Attendees will gain a practical understanding of state-of-the-art testing techniques, emerging AI-driven test solutions, and future trends that are shaping the test ecosystem for advanced 2.5D and 3D chiplet-based semiconductor systems.



Maheedhar Jalasutram
Google



Jeren Ku
Google



Daejin Shin
Google

Maheedhar Jalasutram leads DFT Architecture within Google's Silicon team, where he is responsible for developing scalable test architectures that balance quality, coverage, and test cost for advanced mobile SoCs. Throughout his career, including leadership roles at Google and Texas Instruments, he has driven innovations in concurrent testing, design-for-debug, high-speed test methodologies, and system-level test enablement. His extensive experience spanning DFT architecture, validation, and production test has provided him with deep insight into the challenges of delivering high-quality silicon at scale. This expertise enables him to offer a unique perspective on how test methodologies can be integrated across the entire product lifecycle to improve both quality and manufacturing efficiency.

Jeren Ku leads the Foundry, Assembly Process, and Yield Engineering team within Google's Custom Silicon Operations organization. He oversees manufacturing operations, yield improvement, process optimization, quality management, and product ramp activities for Google's custom silicon programs. Prior to Google, he held leadership positions at Intel and TSMC, focusing on advanced semiconductor process technologies, including FinFET and Gate-All-Around transistor development. His experience across process technology development, manufacturing operations, and yield engineering has given him a comprehensive understanding of how design, fabrication, and production data interact to influence product quality. This background provides valuable insight into building closed-loop methodologies that accelerate yield learning and production readiness.

Daejin Shin leads the Product Engineering and Quality team within Google's Custom Silicon Operations organization, overseeing test yield analysis, manufacturing operations, supply chain quality, and OSAT engagement for multiple generations of Google silicon products. His team plays a key role in delivering scalable, high-quality semiconductor solutions while driving operational excellence across the manufacturing ecosystem. Through his work at the intersection of product engineering, quality management, and high-volume manufacturing, he has developed deep expertise in leveraging test and yield data to improve product robustness and production efficiency. His experience provides valuable perspectives on establishing effective feedback loops between design, test, and manufacturing to achieve world-class quality outcomes.

Testing Chiplet-Based 2.5D/3D ICs : An Academia/Industry perspective

Abstract

As semiconductor products become increasingly complex and quality expectations continue to rise, achieving ultra-low DPPM while maintaining aggressive cost targets requires tighter integration between design, test, and manufacturing. This tutorial explores the concept of Closed Loop Test Engineering, demonstrating how Design-for-Test and Volume Product Engineering can work together to optimize product quality, yield, and test efficiency throughout the silicon lifecycle. Covering topics such as advanced DFT architectures, fault coverage strategies, yield analysis, test optimization, diagnosis methodologies, and production feedback mechanisms, the session provides a comprehensive framework for connecting design decisions with manufacturing outcomes to drive continuous improvement from silicon development through mass production.

Machine Learning is Inevitable or Not: A DFT Designer's View



Ankush Srivastava
Qualcomm

Ankush Srivastava is a semiconductor test expert with over 19 years of industry experience and currently leads the development of advanced Design-for-Test methodologies for Qualcomm's cutting-edge SoCs. Holding a doctorate from IIT Bombay and a degree from BITS Pilani, he has made significant contributions to semiconductor test technology through numerous patents, technical publications, intellectual property developments, and presentations at leading international conferences.

His extensive work in DFT automation, test optimization, and next-generation validation methodologies has given him deep insight into the evolving intersection of machine learning and semiconductor testing. As an active contributor to the global test community through organizations such as ITC, ATS, VLSI Design, and VDAT, Ankush brings a practical and forward-looking perspective on how AI can be effectively leveraged to improve DFT productivity, test quality, and silicon success.

Abstract

Artificial Intelligence and Machine Learning are rapidly transforming engineering workflows across the semiconductor industry, creating both new opportunities and new challenges for Design-for-Test (DFT) engineers. As modern SoCs continue to increase in complexity, traditional DFT methodologies face growing demands for faster turnaround times, improved test quality, lower power consumption, and reduced defective-parts-per-million (DPPM). This tutorial explores the practical application of machine learning in DFT, covering areas such as ATPG optimization, test point insertion, test coverage enhancement, IR-drop analysis, and intelligent DFT automation. It also examines the emerging role of AI-driven assistants and large language models in streamlining DFT workflows, while providing a balanced perspective on where machine learning can deliver meaningful value—and where engineering expertise remains indispensable.

Beyond Scan Dump: Why IEEE P2929 Enables True Scan State Extraction

Principal Product Engineer specializing in new technologies utilizing Tessent Streaming Scan Network. Andy has over 25 years' experience in DFT related product development, 10 years in direct chip design and a MS in Comp Eng from USC. He recently joined the Tessent family in 2025 after 20 years at Cadence Design Systems and has been instrumental in bringing the Scan State Extraction product to market. Andy is currently a member of the IEEE P2929 working group that is driving the Scan/Array Debug Standards.



Andy Hughes
Siemens EDA

Abstract

This tutorial, will cover the details on the new and emerging IEEE P2929 standard and the technology that refines the process of doing a raw dump of scan data into an optimized accurate full functional post-silicon debug Scan state extraction

Testing to Self Testing: Self Test Driven Functional Safety for ISO 26262 Compliant Automotive SoCs



Rajesh Kumar Tiwari
Qualcomm India

Rajesh Kumar Tiwari is Director of Engineering at Qualcomm India, with over 22 years of experience in semiconductor design and Design-for-Test technologies. Over the course of his career at Qualcomm and Texas Instruments, he has led the development of advanced DFT architectures, in-system BIST solutions, and test methodologies across mobile, compute, and automotive platforms. He is also an active contributor to the semiconductor test community through his involvement with IEEE initiatives and technical innovations.

His extensive experience in deploying self-test and safety-focused DFT solutions for complex SoCs has given him deep insight into the challenges of achieving functional safety in modern automotive systems. This expertise positions him uniquely to discuss the evolving role of self-test technologies in enabling ISO 26262-compliant semiconductor designs.



Mohammed Zuber P Malek
Qualcomm India

Mohammed Zuber P Malek is a Senior Staff Engineer and Manager at Qualcomm India with more than 17 years of experience in Design-for-Testability. Having contributed to over twenty successful chip tape-outs, he has developed extensive expertise across in-system BIST, scan synthesis, ATPG, low-power testing, TestSTA, and RTL-level DFT integration. He currently leads Qualcomm's Auto-DFT methodology and TestSTA initiatives, driving scalable and robust test solutions for advanced SoC programs.

His work in architecting automated DFT methodologies and self-test infrastructures for complex silicon platforms has provided him with valuable insight into the intersection of functional safety, diagnostics, and test automation. This experience enables him to offer practical perspectives on leveraging self-test technologies to meet the reliability and compliance requirements of next-generation automotive systems.

Abstract

As automotive systems evolve into software-defined, safety-critical computing platforms, ensuring functional safety throughout a vehicle's lifecycle has become a fundamental requirement. Traditional manufacturing and validation testing alone are no longer sufficient to meet the stringent demands of ISO 26262 compliance. This tutorial explores how Built-In Self-Test (BIST) technologies are transforming functional safety architectures by enabling continuous in-field fault detection, diagnostics, and reliability monitoring. Covering logic BIST, memory BIST, mission-mode testing, and safety-driven test strategies, the session provides practical insights into designing scalable, standards-compliant automotive SoCs capable of delivering robust safety assurance from silicon to system.

The Seamless Integration of Packetized Scan and In-System Test with Advanced ATE Equipment



Lee Harrison
Siemens EDA

Lee Harrison is Director, Product Marketing, with Siemens Tessent Division. He has over 25 years of industry experience working with Siemens Tessent DFT products, with a focus on safety and security, Lee is working to ensure that current and future DFT requirements of Siemens's Automotive and HPC customers are understood and met. Lee Received his BEng in MicroElectronic Engineering from Brunel University London in 1996.



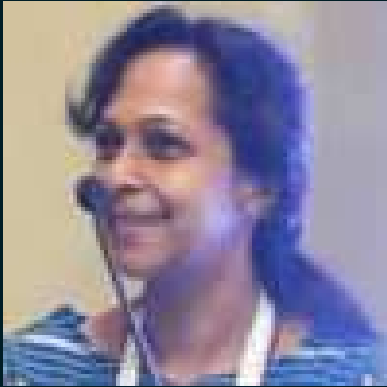
Hagen Goller
Advantest

Hagen started his work career in 1997 and moved into Semiconductor Test in 2001. Since then, he has held various positions in Application Support, Marketing and R&D around the Advantest V93k ATE Platform. Currently he is a technical director in product marketing, looking into new test methodologies and solutions for both ATE and SLT.

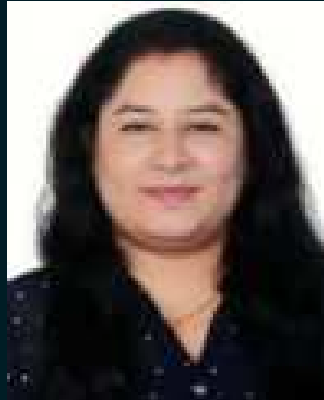
Abstract

As semiconductor devices continue to increase in complexity, reducing test cost while maintaining high quality and reliability has become a key industry challenge. Emerging technologies such as packetized scan architectures and in-system test methodologies are transforming how structural tests are delivered, enabling more efficient use of Automatic Test Equipment (ATE), reducing test data volume, and extending test capabilities beyond manufacturing into system-level and in-field environments. This tutorial provides an overview of packetized ATPG data generation, configuration, and deployment, highlighting how seamless integration with advanced ATE platforms supports scalable test delivery, enhanced diagnostics, data logging, and long-term product reliability throughout the silicon lifecycle.

Advanced Test Data Analytics for Yield and Quality Improvement



Shamitha Rao
Synopsys, India



Sagar Kumar
Cadence



Navya Rastogi
Synopsys

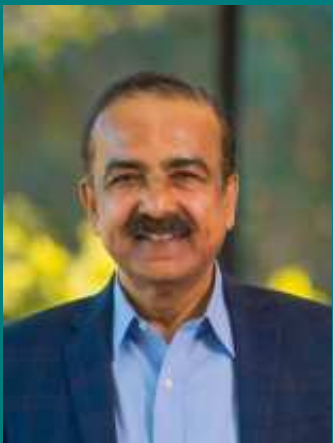


Soumya Mittal
Qualcomm

Abstract

As semiconductor technologies continue to scale and heterogeneous integration becomes increasingly prevalent, the volume and complexity of test and manufacturing data have grown exponentially. Extracting actionable insights from this data has become essential for accelerating yield ramp, improving product quality, reducing scrap, and enhancing manufacturing efficiency. This tutorial explores modern data analytics methodologies within the Silicon Lifecycle Management (SLM) framework, covering advanced statistical techniques, machine learning applications, root-cause analysis, yield monitoring, and real-time quality management. Attendees will gain practical insights into leveraging both local and cloud-based analytics platforms to transform vast semiconductor test datasets into data-driven decisions that improve yield, reliability, and operational excellence.

Understanding Test Escapes and the Limitations of Scan DFT Testing



Adit D. Singh
Auburn University

Adit D. Singh is the Godbold Endowed Chair in Electrical and Computer Engineering at Auburn University and a globally recognized authority in VLSI test, reliability, and semiconductor quality. Over a distinguished academic and research career spanning more than four decades, he has made pioneering contributions to defect-based testing, adaptive testing, and statistical methods for integrated circuit validation. A Life Fellow of IEEE, he has authored more than 300 technical publications, holds internationally licensed patents, and has served in numerous leadership roles across the global semiconductor test community.

His extensive research, industry collaborations, and deep involvement in advancing test methodologies have provided him with unparalleled insight into the challenges of test escapes and timing-related failures in modern semiconductor devices. Combining rigorous academic research with practical industry perspectives, he brings a uniquely authoritative view on improving test effectiveness and ensuring reliable operation of increasingly complex integrated circuits.

Abstract

As semiconductor devices continue to scale in complexity and performance, test escapes have emerged as a critical challenge impacting product quality and system reliability. Despite advances in scan-based testing, cell-aware methodologies, and system-level test strategies, timing-related defects continue to evade detection, leading to operational failures and, in some cases, silent data Corruption in large-scale computing environments. This tutorial provides a comprehensive examination of the root causes behind test escapes, the limitations of existing scan and system-level test methodologies, and the effectiveness of emerging timing-aware test approaches. Drawing on industrial production data and recent research, the session offers valuable insights into improving defect detection, enhancing test quality, and addressing the growing reliability challenges associated with advanced semiconductor technologies.

Scalable ATE Hardware Design: From Concept to Manufacturing with Reusable Architecture



Lokapriya Balakrishnan
Caliber Interconnects

Lokapriya Balakrishnan is a Test Engineer at Caliber Interconnects with over seven years of experience in semiconductor testing and ATE interface hardware development. Her work spans turnkey load board and probe card design, signal and power integrity optimization, device testing, and tester platform conversion projects. In addition to her technical contributions, she has successfully led engineering teams in delivering high-quality hardware solutions within demanding development schedules. Her experience across both hardware development and semiconductor validation provides her with a unique perspective on the challenges of designing scalable, high-performance ATE solutions. This expertise enables her to bridge the gap between hardware architecture, test requirements, and manufacturing realities.



Senthilkumar Dhamodharan
Caliber Interconnects

Senthilkumar Dhamodharan is Vice-President of Semiconductor Test Engineering at Caliber, where he leads the Test Engineering Division responsible for validating SoC, PMIC, Digital, Mixed-Signal, and RF products across ATE and bench platforms. With over 19 years of experience at industry leaders including Qualcomm, AMD, and NXP, he has built deep expertise in semiconductor test, physical design, DFT, and high-volume manufacturing. He also drives strategic initiatives in intellectual property development and leads a high-performance engineering organization of more than 250 test engineers. He holds a Master's degree in VLSI Design from Anna University.



Dyaneswaran Anguraj
Caliber Interconnects

Dyaneswaran Anguraj is currently serving as a Test Engineer at Caliber Interconnect Solutions and possesses over 19 years of diverse experience spanning both academia and the semiconductor industry, with deep expertise in PCB CAM, PCB design, and advanced semiconductor test engineering. He holds a Master's degree in Applied Electronics and began his career with a focus on PCB design, specializing in layout development, signal integrity, and manufacturing support. He later transitioned into academia, serving as an Assistant Professor at reputed engineering institutions, where he mentored future engineers, led impactful research initiatives, and contributed to peer-reviewed publications. Currently, he works as a Test Engineer at Caliber Interconnects, where he focuses on the validation and characterization of digital, mixed-signal, and memory ICs. He has hands-on experience with leading ATE platforms supporting both engineering debug and high-volume production test development.

Abstract

As semiconductor devices continue to push the boundaries of speed, power, and integration, the complexity of Automated Test Equipment (ATE) hardware design has increased significantly. Achieving reliable signal and power integrity while maintaining scalability, cost efficiency, and rapid deployment is now a critical requirement for successful device validation. This tutorial presents a comprehensive approach to designing robust ATE hardware, covering Device Interface Boards (DIBs), SI/PI methodologies, simulation-driven design practices, manufacturing readiness, and validation workflows. A key focus is the adoption of reusable hardware architectures based on modular motherboard-daughtercard concepts, enabling faster development cycles, improved scalability, and enhanced first-time-right success across diverse semiconductor product families.

Customer Centric Post Silicon Validation Approach for System on Chip (SoC)



Ravishankar Manishankar
Intel

Ravishankar Manishankar is a validation expert at Intel with over 21 years of experience spanning System-on-Chip platform validation, functional validation, and embedded wireless software development. Throughout his career, he has worked extensively in areas including PCIe, CXL, customer platform validation, benchmark enablement, and DSP firmware systems engineering across 2G, 3G, 4G, and DAB technologies. He also brings valuable academic experience from the United States, where he conducted research and taught advanced wireless communication topics. His extensive background across silicon validation, software development, and customer platform enablement has provided him with a holistic understanding of the challenges involved in bringing complex SoCs to market. This combination of technical depth and real-world deployment experience gives him unique insight into customer-centric post-silicon validation methodologies and the tools, processes, and strategies required to ensure successful silicon qualification and deployment.



Siloni Palani
Intel

Siloni Palani is a validation engineer at Intel with over nine years of experience in pre-silicon and post-silicon validation for data center GPUs and complex SoCs. Her expertise spans concurrency testing, platform validation, LPDDR5 memory systems, validation tool development, and automation frameworks. She has played a key role in hardware bring-up activities and system-level validation efforts focused on enhancing product quality and debug efficiency. Through her work on complex silicon platforms, validation infrastructure, and automation-driven workflows, she has developed deep expertise in identifying, diagnosing, and resolving system-level issues throughout the product lifecycle. Her experience provides valuable perspectives on modern validation practices and the importance of scalable, customer-focused approaches to post-silicon validation in increasingly sophisticated semiconductor systems.

Abstract

As System-on-Chip (SoC) designs become increasingly complex, ensuring reliable silicon deployment requires a comprehensive validation strategy that extends well beyond fabrication and pre-silicon verification. Post-Silicon Validation (PSV) plays a critical role in bridging the gap between design intent and real-world customer usage, enabling early issue detection, efficient debug, and improved product quality. This tutorial provides a practical overview of customer-centric PSV methodologies, covering silicon bring-up, design-for-debug infrastructure, validation planning, benchmark-driven testing, and unified software frameworks that support both pre- and post-silicon environments. Attendees will gain insights into industry-standard validation flows, debug techniques, and test reuse strategies that accelerate product readiness while improving system reliability and customer experience.



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5	Siemens
6	Google
7	Google
8	Qualcomm
9	Synopsys
10	Amazon
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12	Solitontech
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14	Mirafra
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TECHNICAL PAPER

RL-Driven 3D Clustering of JScan Architecture with Routing and Area Optimization in Chiplet SiP

Hilay Patel

Naman Kalra

Jaynarayan T Tudu

Abstract

Three-dimensional stacked ICs introduce new Design-for-Test (DfT) challenges due to high power density, routing congestion, and cross-tier connectivity constraints. In this work We propose 3D Joint-Scan, a tier-aware DfT architecture that extends the 2D Joint-scan framework to multi-tier 3D ICs and integrates reinforcement-learning-based (RL) physical-design optimization. Each tier combines clustered P-serial (MSS) and Prandom (PRAS) scan structures with dual MISRs. We introduce RL driven scan flip-flops clustering in each layer to learn an optimal configuration to jointly minimize routing congestion and wire length while keeping the test power, test time, and data volume unchanged as base line. Experiments on scaled ISCAS89 benchmarks validate the proposed formulation to be efficient in dealing with routing congestion and area optimization. The design for test parameters such as test time, data volume, and test power are constrained within the given limits. The experimental results show the routing congestion reduction by 38% compared to the base line 2D and 3D JScan architecture. The complete 4-tier design is fully synthesized and place-and-routed in 65 nm technology with a maximum area reduction of 20% compared to baseline.

TECHNICAL PAPER

A Methodology for Robust Testing of Through Glass Vias (TGV) on Glass Substrate-based 3D Chiplets

Manisha Kumari

Jaynarayan T Tudu

Binod Kumar

Abstract

The continued performance pull from the next generation application is driving newer packaging technology to keep up with More-than-Moore performance requirement. Glass substrate-based packaging for the 3D/2.5D chiplet SiP (system in package) is a promising solution which is already in the production pipeline. For 3D/2.5D chiplet packaging technology, through glass vias (TGVs) play a crucial role to interconnect the packaging layers. This layer formation process requires KnownGood-X for substrate, interposer and redistribution layer (RDL). In this work, we address the problem of electrical testing of TGVs for early Known-Good-RDL and Known-Good-Interposer decision. We propose a two-dimensional daisy-chain (2D2C) algorithm and fault localization methodology to test for resistive defects. The experimental results indicate that the proposed methodology detects defects and isolates the defective TGV with a detection rate $> 93.3 - 100\%$. Additionally, the experimental results demonstrate $77.4\% - 100\%$ fault localization.

TECHNICAL PAPER

Cost Aware Sector Symmetry and Wafer Cutting Methods for 3D ICs with Heterogeneous Defects

Tanusree Kaibartta

Digvijay Anand Anand

Saksham Jha

Debesh Das

Abstract

In the growing field of semiconductor technology three dimensional ICS plays a pivotal role due to their potential for enhanced device performance and reduced footprint. However, wafer on wafer stacking faces the challenge of low compound yield due to defect accumulation across layers. To resolve this issue a comprehensive cost analysis is proposed which considers manufacturing, testing and packaging expenses across all stacking layers. In this regard a sector-based wafer manipulation method (SSC4)(where rotationally symmetric wafers are divided into four identical sectors and optimally aligned to improve stacking yield) was introduced. Based on that foundation, this work introduces an extended cost model that incorporates pattern-dependent wafer premiums—accounting for differences in defect quality by assigning varying cost multipliers to different wafer types. This enables finer-grained analysis of stacking decisions in heterogeneous wafer scenarios, where mixing patterns introduce trade-offs between cost and yield.

TECHNICAL PAPER

Innovative Memory Interconnect Architecture: Setting New Standards for Security, Safety and Performance in Real-Time Control MCUs

Prasanth Viswanathan Pillai

Labeeb K

Ramakrishna Pidaparthi

Varshashree Kottadamane

Naveen Kothuri

Rohit Chaudhari

Saya Goud Langadi

Narendra Ravilla

Sivareddy Maramreddy

Abstract

This paper presents an innovative memory interconnect architecture for modern Microcontroller Units (MCUs), addressing the critical triad of performance, safety, and security requirements in embedded systems. The architecture incorporates advanced features including sophisticated control peripherals, non-volatile memory (NVM), static randomaccess memory (SRAM), and efficient interconnect topologies such as crossbar and hierarchical bus structures. Safety mechanisms like Error Correction Codes (ECC) and Memory Protection Units (MPUs) are integrated to ensure fault tolerance. Security features encompass secure boot processes, hardware-accelerated cryptographic engines, and robust access control mechanisms. The paper details the implementation of these features in an emerging real-time MCU platform, demonstrating how the architecture balances performance optimization with safety and security requirements while maintaining cost-effectiveness.

TECHNICAL PAPER

Test Pattern-Driven Detection of Hardware Trojans Using Switching Activity Analysis in FPGA-Based Systems

Kannan S J

Chinakaku Lakshmi Prasanna

Sobhit Saxena

Abstract

Hardware Trojans (HTs) implanted at the RTL level have been identified as a significant security risk, as their low-probability triggering events make them difficult to detect through conventional functional test and ATPG methods. Current side-channel detection methods rely on reference chips, off-chip instrumentation, or computational overhead, making them impractical for field deployment. This paper proposes a synthesizable test pattern-driven detection method based on on-chip switching activity analysis. A parameterized test pattern generator is designed with dual modes: normal mode generates test patterns based on a Linear Feedback Shift Register (LFSR) for pseudo-random pattern testing, whereas test-driven mode generates deterministic test patterns for Trojan detection, ensuring detection of rare combinational, sequential FSMbased, and data leakage Trojan triggers. A cycle-accurate Hamming distance calculation module is used to calculate output divergence between consecutive cycles and compare it with a statistical reference value of six toggle counts. The synthesizability of the test pattern generator and detection logic was validated on a Xilinx Artix7 FPGA (XC7A35T-1CPG236C), achieving 100% detection of all three classes of HTs within 5-16 clock cycles, zero false positives within 6,400 random test cycles, a maximum frequency of 320 MHz, and a total overhead of 178 LUTs and 96 FFs

TECHNICAL PAPER

STAMP: Statistical Trojan Attribution via Multi-class Power-trace analysis

Senthilkumar Dhamodharan

Sinthanai Selvi G

Karthika R

Abirami Vinayagamoorthy

Abstract

The globalization of semiconductor supply chains has posed significant security threats. An attacker can place unauthorized modifications, known as Hardware Trojans (HTs), during the fabrication process or shipping. Once inside the system, the Trojan horses can compromise the secrecy of the keys, disable vital systems, or establish backdoors. The majority of the existing techniques can detect the presence of the Trojan but fail to detect the type of Trojan. This paper introduces an innovative system that is easy to comprehend, capable of detecting the type of Trojan present in the system. It utilizes 26 basic statistical attributes such as mean, standard deviation, maximum, minimum, skewness, and kurtosis from the power consumption patterns of the chip. The dataset consists of power and electromagnetic side-channel measurements of 12 AES Trojan horse benchmark designs (AEST400 to AES-T2000), from IEEE Dataport. The accuracy of the machine learning model, which is based on the XGBoost algorithm, in determining the type of Trojan present is around 77%, thus eliminating the need for a Golden Reference Chip. Furthermore, SHAP analysis is used to obtain a clear “Trojan Fingerprint Map.” The map illustrates precisely which features of the power signal make each type of Trojan unique, considering three different operating conditions. For the first time, this framework allows us to obtain a signal-level fingerprint for each Hardware Trojan variant. This can prove useful in targeted inspection, tracing the origins of the threat in the semiconductor supply chain

TECHNICAL PAPER

Comprehensive Coverage Framework for LPDDR6 Feature Validation: Navigating Complex Modes and Reducing the Verification Closure Gap

Dharini Subashchandran

Meghna Ahuja

Gruhesh Patel

Shyam Sharma

Abstract

LPDDR6's are a breakout DRAM with advanced features -Efficiency Mode, Meta Data on Data Bus, X6 Mode, System Meta Mode including carved-out memory, PRAC, dynamic frequency scaling just to name few - create complex verification challenges beyond traditional Commands, data, Timings, Registers, and DRAM state machine coverage. Feature interactions and configuration-dependent behaviors generate exponential scenario spaces that conventional approaches do not adequately address. This paper presents a feature-centric coverage framework employing Randomization to generate targeted bins across mode transitions, operating speeds, bus width, and density variations. Our coverage framework leverages some of the in-house AI tools to parse specifications and detect coverage gaps which are used for targeted testcase creation. This methodology significantly improves coverage closure and reduces manual effort, providing a scalable solution to validate complex next-generation memory protocols.

TECHNICAL PAPER

A Novel Verification Method for Debug Tracing-in Close Chassis System

Maneesh Pandey

Madhav Lekkala

Abstract

Design for Debug (DFD) plays a crucial role in postsilicon validation during silicon execution, serving as a pivotal phase in the system design cycle. This phase aims to capture design bugs that have escaped detection during the pre-silicon verification phase, particularly in modern complex System-onChip (SoC) designs. In the realm of pre-silicon simulation, DFD SoC presents a dual-faceted approach to validating the SoC, offering both open and closed-chassis debug platforms. In these platforms, trace data is collected at the General-Purpose Input/Output (GPIO) pins and via the GPIO pins to the I3C Bus Functional Model (BFM), respectively. Legacy simulation-based methods for pre-silicon validation have been inherently timeconsuming (3-5 days) due to the necessity of configuring multiple BFMs, such as Sideband and JTAG, within the verification environment. These methods often lead to significant delays and dependencies, complicating the verification process. To address these challenges, we propose a novel verification methodology for debugging trace data in a closed-chassis DFD SoC system. Our proposed methodology leverages the Sneak-Peek (SNPK) engine protocol and Test Access Port (TAP) to perform debugging and tracing of the original source data through the I3C BFM alone, eliminating the need for Sideband and JTAG BFMs. This approach significantly reduces the number of BFM dependencies in the closed-loop chassis debug system, streamlining the verification process and requiring only 1 day for testbench setup bring-up which further enhances efficiency, and effort in bringing up sideband network, validating it for connectivity issues are all a time consuming process, this can be avoided By implementing this alternative method, we aim to accelerate the overall validation cycle, improve deliverables, and contribute to a faster time-to-market for complex SoC products. This methodology not only simplifies the configuration process but also ensures comprehensive tracing of debug data, making it a standalone, portable solution ready for deployment across various SoC project environments

TECHNICAL PAPER

Assertion Based Formal Verification of AES 128 Crypto Core

Shivang Sharma

Vineeth Jaisal

Prashant Singh

Abstract

The Advanced Encryption Standard (AES) is a cryptographic symmetric key algorithm widely used in secure communication, storage devices, and embedded systems. Even a small RTL bug can compromise system security, making its correct implementation critical. This paper presents the formal verification of an open-source AES 128 encryption core using a System Verilog Assertions (SVA) based formal verification environment developed entirely from scratch. The verification environment attaches to the design under test via the System Verilog bind construct, requiring no modification to the underlying RTL. The environment is structured across four verification layers: FSM transition correctness, round register integrity, handshaking signal protocol and per-round datapath correctness. Formal verification provides mathematical guarantee of correctness for all possible states, whereas simulation-based approaches face difficulty in covering all input combination pairs of plaintext and keys. All assertions are formally proven, all cover properties are witnessed, and complete formal sign off is achieved with 100% observability coverage, 99.6% reachability coverage, and 100% sign-off coverage within 278 seconds of total CPU time, confirming mathematical correctness of the AES-128 implementation across every possible plaintext and key combination.

TECHNICAL PAPER

Physically Aware Weighted Fault Model : A new paradigm in testing

Sandipan Sharma

Srinivas Vooka

Maheedhar Jalasutram

Pranav Murthy

Chieh-Jen Ku

Yanhan Zhu

Abstract

For past six decades, standard fault models such as Transition-Delay Faults (TDF) and Stuck-at Faults (SAF) have relied on uniform weighting for fault sites/nodes, despite the common knowledge among Design-For-Test (DFT) engineers that failure probabilities vary across different fault nodes. This reliance on imprecise mechanisms, driven by the historical absence of a scientific weighting methodology, explains the poor correlation between test coverage and physical metrics like yield loss or Defective-parts-per-million (DPPM). While cell-aware testing offers a partial solution, it remains limited by its lack of integration with real-world failure data and its failure to account for routing-related defects. To overcome these challenges, our paper introduces a novel Multi-Layer Perceptron (MLP) network model that utilizes feature correlation buildup to assign accurate failure weightages based on the actual physical parameters, such as metal routing length and total via counts, derived from Continue-on-Fail (CoF) ATE data. As the model is trained on increasing volumes of data, its ability to predict DPPM and fallout will improve, allowing for a more authentic representation of test coverage. Ultimately, this weighted approach enables the optimization of test processes by reducing pattern counts and prioritizing patterns based on their true defect-catching efficacy

TECHNICAL PAPER

Rethinking RTL DFT: A Discrete RTL Flow for Parallel DFT Integration

Mohan Raj Gopal

Veejaye Panayadian

Kundan Jha

Abstract

Shift-left DFT methodologies enable early insertion of test logic at the RTL stage, but conventional flows rely on DFT EDA tools to directly insert CODECs, TDRs, MBIST, scan routers, pin multiplexing, boundary scan, and TAP controllers into design RTL, enforcing serial workflows between design and DFT teams, resulting in high tool runtime, license usage, and intrusive design RTL modifications. This paper presents a discrete RTL DFT flow enabling true parallel development at two levels: design–DFT team independence and concurrent wrapper development. Using script-based, modular grey-box abstractions—TestWrap, MemWrap, and IPWrap—the approach decouples DFT integration from functional RTL and continuous tool invocation. A reusable multi-vendor codec library further reduces tool dependency across partitions and projects. Industrial validation across 50 measured design releases demonstrates an average DFT integration turnaround of 3 days, with a worst-case peak of 11 days, while maintaining functional correctness and achieving scalable, cost-efficient shift-left DFT integration in a representative internal deployment.

TECHNICAL PAPER

A Novel Power-aware ATPG with Biaxial Transition Control for Extreme Low Power Targets

Hanumant Tuntani

Hillol Maity

Sreenu Kakanuri

Peter Wohl

Geguang Miao

Parthajit Bhattacharya

Bruce Xue

Abstract

Aggressive power reduction during compressed scan test is a critical requirement for modern VLSI designs, yet it is fundamentally challenged by compression hardware that obstructs direct ATPG control over scan chain toggles. Prior art has focused on uni-axial power management, providing either horizontal control by freezing the decompressor to hold values across shift cycles, or vertical control by attempting to gate entire scan chains. These solutions, however, operate independently and are often tailored to specific power budgets, with horizontal control typically being more efficient for relaxed targets and vertical control for more stringent constraints. This paper introduces the first co-designed biaxial power control methodology for deterministic ATPG, featuring a novel decompressor architecture that overcomes these limitations. Our hardware enables simultaneous horizontal shift-holding and, direct vertical scan chain blocking through dedicated control registers. This architecture is driven by a tightly-coupled, power-aware ATPG algorithm that intelligently exploits both control mechanisms for highly granular toggle management. The methodology is enhanced by a ‘shift-left’ test generation strategy that embeds power-aware decisions directly into the fault-merging process. Experimental results on industrial designs show that, compared to a baseline uni-axial technique, our complete biaxial solution reduces pattern count by 3.03x, test cycles by 2.16x, and CPU time by 4.73x, while improving test coverage by 3.27%. These gains are achieved while robustly meeting aggressive power targets as low as 15% shift and 5% capture, demonstrating a significant advance in low-power test quality and efficiency.

TECHNICAL PAPER

Differential Evolution with Fitness-and Position-Based Selection in Search of Best Test Pattern for Combinational ATPG

Manish Kumar

Isha Dubey

Priyajit Bhattacharya

Rahul Bhattacharya

Abstract

Evolutionary algorithms (EAs) are demonstrated to be time effective to identify the optimum test pattern with highest fault coverage in a wide search space of digital tests in VLSI circuits. This work focused on developing MATLAB based Automatic Test Pattern Generation (ATPG) framework to determine the optimal test pattern which can detect maximum number of stuck-at faults in combinational circuits using Fitness-and Position-Based Selection Differential Evolution (FPS-DE). In FPS-DE, the parent selection enhances convergence and diversity. The proposed method is evaluated using ITC'99 combinational benchmark circuits and contrasted with Genetic Algorithm (GA), Particle Swarm Optimization (PSO), and a well-known open-source ATPG tool, ATALANTA. The proposed methodology has been used to determine the appropriate mutation strategy for each type of benchmark circuit. Overall, the experimental results demonstrate that FPSDE can effectively generate high-quality test patterns for combinational ATPG

TECHNICAL PAPER

Signal Integrity Simulation Hour Optimization: A Novel AI Framework Using Minute-Scale SI Predictor in High-Speed Test Interface Hardware Design

Senthilkumar Dhamodharan

Dyaneswaran A

Lokendran S

Lokapriya B

Karthika R

Abstract

Signal Integrity (SI) of critical high-speed paths is closely related to topological net connectivity, geometric trace routing morphology, multilayer dielectric stack up permittivity profiles, conductor loss tangent characteristics and via barrel parasitic structures. As high-speed integrated circuit design grows larger, SI simulation becomes computationally unaffordable and machine learning based SI prediction has been explored as a promising solution for freezing layout design without longer simulation hours. In this paper, we present an EDA tool independent, machine learning driven SI prediction framework utilizing heterogeneous Graph Neural Networks (GNNs) for rapid pre-manufacturing integrity assessment. By leveraging standardized PCB manufacturing databases such as ODB++, IPC-2581, and Gerber, the framework enables data extraction and model training from layouts generated by diverse EDA tools. Our methodology constructs attributed heterogeneous graphs encoding electrical adjacency, Euclidean spatial proximity and vertical reference plane coupling through typed edge relations. Thus, we propose a novel graph structure, TL Graph, to unify representations of transmission line structure and fine grained segment relations. Though this framework may require several iterations to achieve compliance, the time line penalty is minimal with sub 3 second inference enabling engineers to adjust layouts with negligible schedule impact versus several 100s of hour cycles. The proposed methodology significantly reduces the overall design time line by utilizing model based predictions in place of multiple iterative EM simulations during the initial design phase, with full wave simulations performed only for final board evaluation. The framework reduces design iterations by 73% and compresses development cycles by 1.8 weeks per platform. The scope of the future research work is also discussed towards the end of this paper.

TECHNICAL PAPER

Post-Silicon Validation of Neuromorphic SoCs: A Hybrid BIST and ML-Based Approach for NVM Synaptic Fault Detection

Kalyana Sundaram
Chandran

Senthilkumar Dhamodharan

Sindhu Mathy S

Abstract

Neuromorphic Integrated Circuits (ICs) emulate biological neural systems through event-driven spike processing, enabling edge AI, robotics and cognitive computing. Post-silicon validation of these systems faces critical challenges due to absent on-chip debug infrastructure, limited observability into asynchronous spike-driven operations and large-scale synaptic connectivity. Non-Volatile Memory (NVM) synapses are prone to drift, wear-out and stuck faults that degrade inference accuracy. Existing approaches BIST, inference-based testing, and simulation struggle with intermittent faults arising from analog variability and asynchronous operation. This paper presents a hybrid data-driven framework combining structured BIST sequences, adaptive stress patterns and lightweight ML runtime monitors with hierarchical fault localization at neuron, synapse and network levels, correlating spike activity statistics, synaptic state inference and telemetry data. Silicon validation on a fabricated 28 nm CMOS neuromorphic processor (1024 LIF neurons, 50 chips, 5 fabrication lots) demonstrates $94.2\% \pm 1.8\%$ fault coverage, 92% diagnostic time reduction versus exhaustive scan and robust operation under 18% analog variation. Total overhead is 1.3% die area and 2.3% power significantly lower than DiagNNose with statistical significance versus BIST-only ($p < 0.001$), confirming scalable, resilient validation for mission-critical neuromorphic systems

TECHNICAL PAPER

T-MAP: A Cross-Platform AI driven Test-Program Metadata Analysis Tool for Digital Coverage, Force, limit and Range Verification

Kaushik Chakravorty

Vishal Rohilla

Pratyush Dargan

Dundapa Sankapal

Sudhish Raj Gj

Robert Cook

Abstract

Testers across the industry employ diverse digital/analog inputs and generate varied outputs, making a universal audit framework impractical. Automated audits of digital coverage, voltage settings, force conditions, and limit-vsclamp comparisons are becoming essential for every test program. T-MAP extracts input and output information to construct a metadata-analysis model that highlights coverage gaps, reduces manual effort, streamlines Git-PR reviews, and captures errors missed by human auditors. AI-driven analysis ensures scalability as automation scopes expand. The approach is fully agnostic to tester type, input format, and output interface, eliminating the maintenance overhead of platform-specific scripting and improving engineer adaptability across platforms

TECHNICAL PAPER

AI-Driven IP Configuration Optimization for Post-Silicon Validation

Akhilesh Tiwary

Utsav Banerjee

Nihar Chaniyara

Maneesh Kumar Pandey

Abstract

Post-silicon validation of configurable intellectual property suffers from a persistent configuration selection problem: the legal operating space grows rapidly with feature combinations, but actual silicon execution remains limited by platform availability, debug effort, and turnaround cost. In many industrial flows, configuration choice is still driven by manual expertise and retrospective coverage inspection, which makes it difficult to prioritize representative and corner-case scenarios systematically. This paper presents a machine-learning-driven framework for post-silicon IP configuration optimization. The method converts raw configuration descriptors into a behavior-oriented feature space, applies K-Means-family clustering and DBSCAN to identify dense and sparse operating regions, and produces a reduced yet diversity-preserving execution set for post-silicon testing. The workflow is organized as a three-layer system comprising data cleanup, clustering and evaluation, and inference. Progressive experiments show that feature-aware clustering materially improves planning quality: K-Means improves from a silhouette score of 0.3250 to 0.4480 across refinement stages, while DBSCAN improves from 0.0931 to 0.5451 with only about 0.3% noise in the final setting. The proposed framework reduces redundant postsilicon test cycles while preserving representative and high-risk configurations needed for effective validation.

TECHNICAL PAPER

State-Isolated Scan - A Secure Low-Power Scan Architecture

Ravikumar C.P.

Kushal C.

Abstract

The number of flip-flops and gates in Systems-onChip is steadily increasing. Power dissipation during scan shift can exceed the limit imposed by the package, making the test destructive. Power droop resulting from high switching activity during scan test can result in errors, leading to a test-induced yield loss. Several authors have proposed techniques such as staggered scan to reduce scan shift power. Another technique is to add a series of logic gates that block the propagation of switching activity from scan registers into the combinational logic. Scan chains can compromise the security of circuits. A knowledgeable hacker can put the circuit in test mode and scan out sensitive information. In this paper, a technique called “State Isolated Scan” (SIS) is proposed, which addresses both the power issue as well as the security issue. SIS allows complete isolation of the state information during scan shift-in and shift-out operations, thereby eliminating the propagation of cell switching activity into the combinational logic. At the same time, a hacker does not get access to scan data through top-level pins, thereby making the test architecture secure.

TECHNICAL PAPER

eFPGA-Enabled Dynamic Access Control for Secure IEEE 1687 (IJTAG) Networks

Anekait Thampi

Manish Nagaraju

Anshul Raghavendra Katti

Sudeendra Kumar K

Abstract

Modern System on Chip (SoC) designs integrate numerous embedded instruments for testing, debugging, postsilicon validation, and in-field monitoring. The IEEE 1687 (IJTAG) standard provides scalable access through a reconfigurable scan network of Segment Insertion Bits (SIBs), but this flexibility exposes internal resources to unauthorized access through the test infrastructure. Existing protection approaches rely on fixed hardware mechanisms, limiting adaptability across device lifecycle phases. This work proposes a secure IJTAG architecture integrating an eFPGA between the TAP and the IJTAG network as a reconfigurable security layer that controls instrument cluster connectivity through authenticated configuration, enabling lifecycle-aware isolation while preserving IJTAG flexibility. The architecture is evaluated on IJTAG benchmark networks to assess scalability.

TECHNICAL PAPER

Design of a SAT-Resilient IJTAG Architecture for Secure and Scalable On-Chip Instrument Access

Saravanan P

Jothika K

Dharani Sree K

Nivashini S

Sivaprabha Sri Pl

Abstract

The IEEE P1687 Internal JTAG (IJTAG) provides a flexible infrastructure for accessing embedded on-chip instruments used for testing, debugging, and configuration in modern integrated circuits. However, the accessibility of IJTAG scan networks can expose internal circuit structures and sensitive data, making them vulnerable to attacks such as intellectual property theft, reverse engineering, and unauthorized instrument access. Conventional logic locking techniques provide limited protection since they can be compromised using de-obfuscation methods. To address these challenges, this paper proposes a SATresilient secure IJTAG architecture that integrates Fault-based Logic Locking (FLL) for Locked Segment Insertion Bits (LSIBs) with a hybrid Anti-SAT block employing multiplexer-based wire entanglement. The proposed design restricts unauthorized access to embedded instruments while increasing the complexity of key recovery. Experimental results demonstrate that increasing the key width significantly enlarges the key search space; A 16-bit key leaves 24,286 unresolved keys after 10 SAT solver iterations, making brute-force recovery impractical.

TECHNICAL PAPER

PQC-Based Secure Access Manager for IJTAG Network

Sudeendra Kumar K

Abhinav S

Prajwal G S Basavaraj

Arun Kumar N

Abstract

As the complexity of System-on-Chip (SoC) designs is increasing, the number of instruments embedded within the chip has also grown significantly. On the other hand, the flexibility provided by the IEEE 1687 standard has led to security issues such as unauthorized access, leakage of information contained in the scan chain, replay attacks, and misuse of the test interface. The existing security schemes for IJTAG are primarily based on conventional cryptographic techniques like RSA and lightweight ciphers. As these techniques are vulnerable and it is safe to migrate to post quantum ciphers even for the chip test security for the devices which have long utilization life especially in the automobiles and industrial control. This work addresses the security issues by developing a secure IJTAG access architecture based on lattice-based Post Quantum Cryptographic (PQC) techniques. The proposed solution is a combination of ML-KEM and ML-DSA for a secure IJTAG. ML-KEM is used for secure session key establishment. ML-DSA is used for authentication of test access requests and unlocking the Access Manager. In comparison to existing schemes, based on classical cryptographic schemes, the authorization time/access time of the proposed PQC based mechanism is high. The security analysis shows that, the proposed scheme is a countermeasure against brute-force and scan sniffing attacks on par with the existing solutions.

TECHNICAL PAPER

Real-Time Path Resistance Compensation and Spatial Diagnostics for High-Volume Wafer Test

Mathangi Raghuraman

Siva Elango S

Dinesh Sharma

Sujith Thomas

Abstract

During high-volume wafer sort on Automated Test Equipment (ATE), DC parametric measurements are frequently degraded by variable contact resistance at the probe needle-to-pad interface. While standard ATE Time Domain Reflectometry (TDR) calibration resolves edge-timing delays, and offline DC calibration effectively reduces static system resistance from the Parametric Measurement Unit and loadboard traces, these methods fail to account for dynamic, touchdown-dependent fluctuations in contact resistance. This uncompensated variance leads to false failures, excessive retesting, and significant yield loss. This paper proposes a real-time de-embedding methodology that dynamically measures the Total Path Resistance for every die. By isolating and compensating for the variable contact resistance component during active testing, the proposed method recovers true silicon performance without throughput penalty. Furthermore, this work introduces a novel spatial diagnostics framework for highvolume wafer test. By aggregating real-time path resistance data into 2-D wafer heatmaps, the system successfully isolates systematic mechanical degradation such as prober planarity tilt enabling data driven predictive hardware maintenance. Silicon validation across high-volume production devices demonstrates tightened measurement distributions, significant yield recovery, and improved probe card lifecycle management.

TECHNICAL PAPER

Polynomial Regression Based Qualitative Assessment of Automated Test Equipment Calibration

Matthias Werner

Ilia Polian

Anand Venkatachalam

Simon Schweizer

Ernst Aderholz

Matthias Sauer

Abstract

In order to preserve measurement accuracy, Automatic Test Equipment (ATE) periodically generates ATE adjustment data as part of its periodic maintenance. Parametric current measurements involving analog and digital instrumentation have been analyzed together with ATE adjustment data using polynomial regression. Key takeaway from this analysis done with CAN Transceiver measurements from multiple Advantest V93000 Tester using multiple test hardware is that degree of correlation between the measurement result and adjustment data varies from channel to channel and it is also dependent on the ATE measurement range. Additional insights on the process capability trend of parametric measurement involving tester channel that shows negative correlation along with time series plots of ATE adjustment data are provided with an aim to evaluate accuracy and drift beyond specification limits in order to derive more value from ATE instrumentation.

TECHNICAL PAPER

A Novel Plug-In Module Architecture for Extending Automatic Test Equipment Capability to Wireless Testing of Pin-Less Semiconductor Devices

**Sathiyapriya
Krishnamoorthy**

Manoj Pachaiyan

Senthilkumar Dhamodharan

Abstract

Contactless integrated circuits are increasingly used in wireless identification, secure transactions, and short-range communication applications. Devices such as Near Field Communication (NFC), Radio Frequency Identification (RFID), smart cards, and secure identification modules operate through electromagnetic coupling using on-chip antenna structures, enabling power harvesting and bidirectional communication without dedicated electrical interfaces. However, production testers such as Advantest and Teradyne are primarily designed for electrical pin-based testing and do not natively support validation of contactless communication behavior. This work proposes a production-compatible wireless validation architecture that enables contactless device characterization within an automated production test environment. The proposed approach integrates a wireless interface on the load board consisting of a radio-frequency stimulus generator, protocol conversion layer, near-field coupling antenna, and signal demodulation receiver synchronized with the tester control framework. This enables automated carrier generation, command modulation, and capture of load-modulated responses from the device under test. Experimental validation was performed using NFC-enabled RFID tag devices across 120 samples. Carrier field detection showed reliable activation above 1.6 A/m, while RF power harvesting generated internal supply voltages between 2.4 V and 2.8 V. Load-modulated responses ranged from 180–240 mV, enabling reliable demodulation and protocol decoding. Command-response operations, including Unique Identifier (UID) read, memory access, and anti-collision, achieved a bit error rate below 10^{-6} with an average communication latency of 3.2 μ s and less than 4% device variation. Results showed over 96% correlation with conventional bench validation, demonstrating the feasibility of scalable production testing of contactless semiconductor devices.

TECHNICAL PAPER

Unified Compact Health and Aging Models for Manufacturing to In-Field Silicon Quality and Reliability Management

Dan Alexandrescu

Shubharthi Datta

Leela Krishna Thota

Abstract

Analytics of Silicon Lifecycle Management (SLM) monitors measurements provides the deep silicon metrics and insights required for the semiconductor lifecycle, from manufacturing test to in field operation. This paper presents a solution for preparing compact models from monitor measurements to compute health, aging, and remaining useful life (RUL) metrics. A lightweight autoencoder-based health signature provides robust anomaly detection under partial observability, while HTOL calibrated aging model maps measured degradation to circuit performance and RUL, scaled using mission profile acceleration. The compact models are managed and prepared during manufacturing testing and deployed for edge or in system inference, enabling continuous silicon health and reliability analytics at device and fleet levels.

TECHNICAL PAPER

Reliability Refining Next Generation UV Cured Conformal Coatings under Harsh Environment Testing

Aurkie Ray

Andi Duffy

Saskia Hogan

Cole Sandvold

Bethany Turner

Phil Kinner

Christopher Allen

Anna Lifton

Abstract

High reliability electronics pose a higher risk of failure due to the water film formation on the substrate surface when operating in harsh environments such as high temperature and high humidity. This has drawn attention to electronic industries. Typical electronic manufacturing processes potentially add ionic contamination to the substrate surface which could lead to failure in presence of high temperature and high humidity with a working bias voltage. These failures result in an increase of leakage currents, electrochemical migration and corrosion which further result in degradation in performance. To keep a check on these failures the use of conformal coating on the PCB is increasing with time. The electrochemical reliability inferred from the Surface Insulation Resistance (SIR) test helps to access the compatibility of conformal coatings with flux chemistries under harsh environment. This study was focused on assessing the effect of two different generations of UV curing conformal coating on protecting PCBs built with various solder pastes. The effect of solder paste chemistry, preconditioning of the boards before SIR testing (isothermal aging and pre thermocycling) was studied. A customized condensation test protocol is designed to create harsh environment to screen conformal coatings for their ability to withstand moisture ingress and protect the assembly from moisture-related failures such as corrosion and dendritic growth formations. Such study can result in improved electrical reliability and identify the optimal material set and process parameters for operation in harsh environments.

TECHNICAL PAPER

Design and Context Aware Embedded Monitor Analytics Through High-Volume Algorithmics and Explainable AI

Dan Alexandrescu

Shubharthi Datta

Leela Krishna Thota

Abstract

Silicon test results are highly dependent on operating voltage, temperature, and design intent, yet are often interpreted without full context. This paper presents an approach that merges test measurements, operating conditions reported by embedded Silicon Lifecycle Management (SLM) voltage and temperature monitors, and design expectations to enable context aware interpretation of silicon results. Algorithms and explainable AI techniques guide engineers directly to the dominant contributors of misalignment, replacing manual chart inspection with automated, data driven insight generation, distinguishing process variability, systematic model to silicon correlation gaps, and true outlier parts and enabling data driven decisions across NPI, yield ramp, and highvolume manufacturing.

TECHNICAL PAPER

Physical Design Aware Verification Methodology for Closing Coverage Gaps in SharedBus MBIST

Shivam Tulsyan

Prachi Sinha

Maheedhar Jalasutram

Mayank Parasrampuria

Vasudevan Pillai A

Abstract

The industry shift toward SharedBus MBIST architectures has successfully mitigated the Power, Performance, and Area (PPA) bottlenecks associated with traditional embedded memory testing. However, reusing functional paths for testing introduces severe verification challenges, as conventional MBIST algorithms often fail to detect intricate mapping errors like data-bus scrambling, tied-off data bits, and irregular address bits decoding. If left undetected, these discrepancies in implementation result in silent coverage gaps and ineffective memory repair mechanisms. This paper proposes a robust assertion-based RTL verification methodology specifically designed to close these gaps in SharedBus MBIST implementations. By deploying a Walking-0 pattern and continuous monitors across SharedBus and physical memory interfaces, the methodology enforces a strict set of verification rules. Experimental results validate this approach, demonstrating the successful identification of critical implementation bugs across multiple vendor cores that escaped conventional verification. The paper concludes by proving that the overhead of this methodology is minimal and highly justified by the resulting improvements in silicon quality.

TECHNICAL PAPER

Constraint-Based Functional Testing of Encrypted Memory Systems

Ravikumar C.P.

Abstract

Encrypted memories which make use of encryption standards such as AES-128 are becoming common in applications such as artificial intelligence, automotive/industrial electronics. Conventional testing schemes, such as Marching Tests, are inadequate for testing of encrypted memories since they do not test the encryption/decryption logic. Further, traditional tests read/write individual bits, whereas AES-128 standard encrypts chunks of 128 bits. This paper proposes test algorithms which can be used both in field testing as well as in factory testing. The essential idea is to write magic squares (MS) and read them back to verify that all properties of the magic square are intact. MS are very sensitive to a single error and a single error in one of the bits can cause many constraints of the MS to fail. We have developed a simulator to verify and benchmark the test algorithm

TECHNICAL PAPER

Enabling EDA Automation for HBM Testing Using A Plug-n-Play DFT Interface

Quoc Phan

Bartosz Zelek

Marta Stępniewska

Anshuman Chandra

Barbara Działowska

Jonathan Gaudet

Abstract

High bandwidth memory (HBM) has emerged as the primary high-speed memory in modern AI computing. It provides an ultra-fast wide and power efficient data transfer for AI accelerators and graphics processing units (GPUs) using innovative 3D stacking and advanced through-silicon-via (TSV) technology. However, HBM 3D stack presents significant test challenges at both wafer-level and post package assembly. Memory cells inside each DRAM stack and the micro-bump interconnect in the logic base die must be thoroughly tested to ensure good quality and yield post bonding. In this paper, we describe an efficient package-level testing flow that enables seamless EDA tool automation for DFT insertion and pattern generation. We present the design of different components that enable plugging of the HBM interface to the IJTAG network and leverage an existing memory BIST controller for both memory and interconnect test.

TECHNICAL PAPER

Enhancements in Memory Test for improved diagnosability and comprehensive multi-bank test

Prachi Sinha

Shivam Tulsyan

Veerabhadrrao Vasa

Mayank Parasrampur

Abstract

The scaling of System-on-Chip (SoC) architectures to sub-5nm nodes necessitates highly optimized custom memory designs. However, these layouts introduce unique physical defect mechanisms and coupling faults invisible to industry-standard March tests. This paper proposes a novel custom testing methodology specifically engineered for multi-bank memory architectures. By implementing a programmable, bank-aware Built-In Self-Test (BIST) architecture, the proposed solution enables concurrent multi-bank stressing to detect inter-bank crosstalk while maintaining strict power-density limits through a custom scheduling algorithm. This methodology provides a scalable framework for ensuring high reliability in performance-critical silicon environments. While the multi-bank BIST identifies the presence of inter-bank coupling, physical localization in sub-5nm nodes requires non-invasive back-side analysis. Our methodology includes a 'Diagnostic Mode' that allows the BIST to loop specific stress patterns, enabling Laser Voltage Probing (LVP) to capture high-resolution internal waveforms. This synergy between custom BIST and optical probing significantly reduces the Time-to-Yield (TTY) by pinpointing the exact physical origin of marginal delay faults. Simulation results demonstrate the effectiveness of this approach in identifying complex inter-bank coupling and providing the deterministic triggering required for failure analysis in advanced process nodes.

TECHNICAL PAPER

A novel hardware design for effective supply voltage glitch injection

Antony Varghese

Ashok Kumar

Asmita Mohapatra

Abstract

Supply Glitch Voltage Injection is one of the effective techniques to analyse and validate a chip's performance and reliability in case of sudden changes in the supply. Conventional functional validation poses unique challenges owing to the difficulty of creating these conditions. This paper elaborates on these challenges and proposes a novel, cost-effective hardware solution that facilitates functional validation of these circuits for devices operating on a supply voltage range of 1.7V to 3.6V. The hardware can control the ramp rates of the generated glitch.

TECHNICAL PAPER

Validation Methodology to Characterize Absolute Propagation Delay, Delay variation over temperature and Programmable Delay of 1ps DNL step in Wideband RF Buffers upto 12.8GHz

Harish Ramesh

Jason Xavier

Pranav Kumar

Abstract

Wide Band RF Fanout Buffers is widely used in markets such as Wireless Infrastructure (Wireless Backhaul, 5G base station Beam forming applications), Aerospace & Defense (Phased Array Radar, Beam Forming), Test & Measurement. Modern Wideband RF Clock buffers and Synthesizers have provision to delay its output clock up to several picoseconds range with a step size of around 1picosecond. There are certain applications where programmable delay steps, propagation delay of buffers and channel to channel skew play a critical role in defining a system which require synchronized clocks across different channels. Customers always look out for min/max variation across PVT to budget their system accordingly. Therefore skew, propagation delay and its variations across temperature becomes a very critical parameter during the characterization phase. These measurements are very challenging and sensitive to setup variations, PCB interconnects, cables and measuring equipment. It also gets challenging at higher frequency where the delay range to be measured is greater than clock time period. In this paper measurement methodologies of Absolute propagation delay measurement, Propagation Delay Variation over temperature (Rate of change of delay with temperature) and Precise analog delay step measurements upto a resolution of 1ps are discussed in details with Si results

TECHNICAL PAPER

DFT-Enhanced Spare Cell Architecture for Scan-Integrated ECO and Leakage Optimization in SoCs

Pramod Gayakwad

Chandhramohan K P

Vishwanath Kunchigi

Raghavendra H D

Khushboo Rathore

Vamsi Krishna Oliveti

Santhosh Kamatam

Abstract

Advanced SoC designs increasingly rely on spare cells to enable post-layout and post-silicon engineering change orders (ECOs). However, conventional spare cell implementations are typically logic-only constructs that are neither scan-aware nor optimized for leakage and decoupling behavior, leading to test coverage challenges and unintended power penalties. This paper presents a DFT-enhanced spare cell module that integrates fullscan capability along with scan-controlled input-state enforcement to enable leakage reduction and effective decoupling utilization during inactive modes. The proposed architecture allows spare cells to be seamlessly incorporated into scan chains without perturbing existing DFT infrastructure, while simultaneously enabling their reuse as functional ECO resources. Analysis across representative design scenarios demonstrates that the proposed spare cell approach improves ECO readiness and scan integration with negligible area overhead and controlled leakage impact. The technique is particularly suitable for advanced technology nodes where unused logic contributes disproportionately to static power and reliability concerns. In representative design-level analysis, the method achieves up to ~98.9% stuck-at fault coverage for the spare module and demonstrates ~15% reduction in spare-logic leakage (~0.75 mW at SoC level).

TECHNICAL PAPER

Hybrid Power Gating: Hardware Trio Framework based ATPG for Low-Power Scan (TRC Paper)

Praveen Raghuraman

Darshan V

Vivek Roopchand

Arul Karthick Kumar

Karthikeyan Soundararajan

Abstract

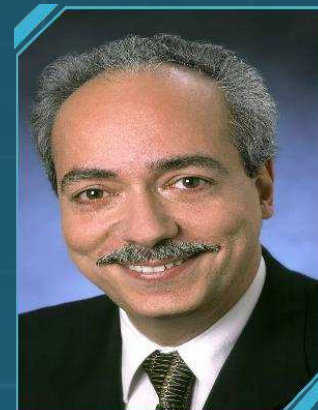
State-of-the-art System-on-Chip (SoC) designs have evolved into highly complex, stacked architectures characterized by massive logic depth, small form factors, and stringent low-power requirements. The drastic scaling of design complexity and product features in cutting-edge SoCs introduces significant challenges, making structural testing using scan indispensable for determining design yield and robustness of a design. Due to recent spike in process node advancements in semiconductor industry, managing the power density during scan testing has become a critical bottleneck. To address these challenges, it is imperative to achieve high quality through test patterns that deliver stable results across different PVT conditions. Simultaneously, reducing the average unit cost and overall test cost requires optimized IR drop resistant test vector set for efficient sequential fault screening across blocks with minimal test time. Excessive switching activity during the ATPG phases lead to voltage droop (IR drop), causing artificial test failures and yield loss. Existing solutions, such as frequency throttling, EDA supported Low Toggle Vectors often result in unacceptable pattern count inflation or test time penalties. This paper addresses the challenges associated with achieving scan test power reduction in such advanced high density SoC designs.

KEYNOTES

1. Designing Chiplets and 3DIC for Quality and Reliability

Bio: President of Synopsys Armenia and Chief Architect and Fellow at Synopsys, and one of the foremost pioneers in semiconductor test, BIST, DFT, and EDA, with prior leadership at Virage Logic, LogicVision, and AT&T Bell Laboratories. He currently serves as President of the IEEE Test Technology Technical Council (TTTC) and founded the IEEE 1500 Standardization Working Group. His work spans 40+ U.S. patents, four books, and 350+ publications, and honors including the IEEE Industrial Pioneer Award and the IEEE TTTC Lifetime Contribution Award.

Abstract: As semiconductor innovation moves beyond traditional transistor scaling, chiplet-based architectures and 3D integrated circuits are emerging as the foundation of next-generation computing systems. While these technologies enable unprecedented levels of performance, scalability, and heterogeneous integration, they also introduce new challenges in test, quality, reliability, and lifecycle management. This keynote explores the design methodologies, DFT strategies, and reliability frameworks required to ensure robust, high-quality chiplet and 3DIC systems, highlighting the critical role of advanced test technologies in enabling the future of semiconductor integration.



SPEAKER

Yervant Zorian
(Synopsys)

2. Silent Data Corruption by 10× Test Escapes Threatens Reliable Computing

Bio: William E. Ayer Endowed Chair Professor at Stanford University and a globally recognized leader in robust computing, system reliability, and electronic design automation. His pioneering research in testing, validation, fault prediction, and resilience has shaped modern semiconductor systems deployed across cloud, AI, and automotive platforms, and his work with academia, industry, and national semiconductor initiatives gives him unique insight into the reliability challenges of next-generation computing.

Abstract: In an era where computing underpins everything from cloud infrastructure and AI autonomous systems, ensuring reliability has never been more critical. This keynote examines the growing threat of test escapes and silent data corruption, highlighting the limitations of conventional testing approaches and the need for next-generation strategies to safeguard trust in increasingly complex semiconductor systems.



SPEAKER

Subhashish Mitra
(Stanford University)

KEYNOTES

3. SI Complexity to AI Revolution: India's Silicon Leap 2047

Bio: Semiconductor engineering leader with nearly two decades in post-silicon validation and high-volume manufacturing test across Digital, Mixed Signal, PMIC, and RF technologies, with leadership roles at Caliber Interconnect Solutions, Qualcomm, AMD, and NXP. His ongoing research in AI/ML for post-silicon validation gives him a distinctive perspective on intelligent, AI-driven testing.

Abstract: As artificial intelligence redefines the semiconductor landscape, intelligent testing, validation, and manufacturing have become essential enablers of innovation. This keynote explores how AI-driven methodologies, digital twins, and ecosystem collaboration can accelerate India's semiconductor journey and strengthen its position in the global technology value chain.



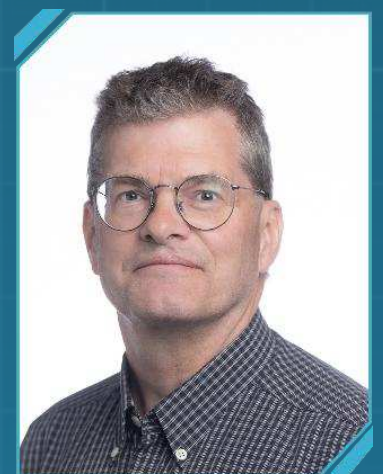
SPEAKER

Senthilkumar Dhamodharan
(Caliber InterconnectSolutions)

4. AI in Test: Fear It or Harness It

Bio: Senior Fellow at AMD, where he has led the DFX Strategy team for 19 years, following 22 years at HP and Agilent Technologies working on DFT and test methodologies. He holds 50 patents, serves on the ITC Steering Committee, and remains active in IEEE working groups — including as Editor for all three IEEE 1687-family standards currently in progress.

Abstract: Artificial Intelligence is rapidly transforming industries worldwide, creating both unprecedented opportunities and significant challenges. In the semiconductor test ecosystem, AI is reshaping how products are designed, validated, and tested, while simultaneously introducing new requirements for ensuring the reliability and trustworthiness of AI-driven systems. This keynote examines the evolving relationship between AI and test, highlighting how the test community plays a critical role in enabling the next generation of intelligent technologies.



SPEAKER

Jeff Rearick
(AMD)

KEYNOTES

5. Built-in Intelligence – Leveraging Advanced DFT for Silicon Health Monitoring

Bio: Vice President of Software Engineering for Tessent Silicon Lifecycle Solutions at Siemens EDA, and a globally recognized expert in semiconductor test and diagnostics. He has pioneered innovations in test compression, Logic BIST, Memory BIST, low-power DFT, and in-field testing (including EDT/TestKompress, VersaPoint Test Points, Observation Scan Technology, and packetized scan-based in-field test). He holds 60+ U.S. patents, 100+ publications, and awards including the IEEE Donald O. Pederson Outstanding Paper Award and the ITC Most Significant Paper Award.

Abstract: As semiconductor technologies continue to evolve, ensuring silicon quality, reliability, and long-term health has become increasingly challenging. Modern designs require test methodologies that extend beyond manufacturing to enable continuous monitoring throughout the product lifecycle. This talk explores how advanced Design-for-Test (DFT) infrastructures provide the foundation for comprehensive silicon health monitoring, integrating on-chip intelligence, diagnostics, and lifecycle analytics to improve test quality, reduce cost, and enhance reliability from manufacturing through field deployment.



SPEAKER
Nilanjan Mukherjee
(Siemens)

6. From Silent Patient to Self-Healing Silicon: The Four Evolutionary Stages of DFT in Mass Production

Bio: Director of Custom Silicon Engineering Operations at Google, where he oversees Tensor manufacturing, test, and quality. Over more than two decades — including leadership roles at Google, Apple, and Altera — he has led the ramp of advanced products from development to high-volume production, spanning FPGAs, SoCs, memory, PMICs, and security devices.

Abstract: As semiconductor devices grow in complexity and production volumes continue to scale, ensuring silicon quality and reliability has become increasingly challenging. This keynote explores the evolution of Design for Testability (DFT) from a traditional diagnostic tool into an intelligent, lifecycle-driven framework that enables improved yield, reliability, and manufacturing efficiency. By examining the four evolutionary stages of DFT, it highlights how modern test methodologies are shaping the future of autonomous and self-healing silicon.



SPEAKER
Bizhan Delgoshaei
(Google)

1. From Point Tools to Agentic AI: How EDA has Impacted the Semiconductor Industry

Speaker: Don Chan (Cadence)

Bio: Vice President of Research and Development at Cadence, where he leads the Foundry organization and oversees technology enablement, process certification, and customer support for advanced nodes, as well as marketing and business development for the Digital and Signoff portfolio. He has led R&D initiatives across 3D-IC, Conformal, Modus, and Stratus technologies, with prior leadership at Synopsys and Fujitsu Micro.

Abstract:

Electronic Design Automation (EDA) has been the driving force behind decades of semiconductor innovation, enabling engineers to design increasingly complex chips while sustaining the pace of Moore's Law. As transistor scaling approaches its physical limits, the industry is transitioning toward heterogeneous chiplet-based architectures, 3D integration, and AI-driven design methodologies. This talk explores the evolution of EDA from traditional point tools to intelligent, agentic AI workflows, highlighting how advances in design technology co-optimization, DFT methodologies, and AI-assisted automation are reshaping semiconductor design. Attendees will gain insights into the next generation of EDA technologies that will power future innovations in high-performance computing and artificial intelligence.



2. The Critical Role of Test Strategy in India's Semiconductor Growth

Speaker: Alpa Sood (Teradyne)

Bio: Country Manager for India at Teradyne, with over 15 years of experience across business, policy, and government affairs. She has worked closely with the Government of India and state governments to grow the semiconductor ecosystem, and previously led government affairs, legal, and strategic policy engagement at Marvell India.

Abstract:

As India accelerates its ambitions of becoming a global semiconductor hub, developing a robust test ecosystem is emerging as a strategic priority. Advanced test methodologies are essential not only for ensuring product quality and reliability but also for strengthening manufacturing capabilities, enabling supply chain resilience, and enhancing global competitiveness. This talk explores the pivotal role of test strategy in building a sustainable semiconductor ecosystem, highlighting the importance of collaboration between industry, government, and academia to support India's vision of becoming a leading semiconductor nation.



3. The Intelligent Silicon Era: Redefining Semiconductor Test Through Innovation, AI, and Collaboration

Speaker : Rajesh Vaddempudi (Advantest, India)

Bio: Vice President of Software Engineering for Tessent Silicon Lifecycle Solutions at Siemens EDA, and a globally recognized expert in semiconductor test and diagnostics. He has pioneered innovations in test compression, Logic BIST, Memory BIST, low-power DFT, and in-field testing (including EDT/TestKompres, VersaPoint Test Points, Observation Scan Technology, and packetized scan-based in-field test). He holds 60+ U.S. patents, 100+ publications, and awards including the IEEE Donald O. Pederson Outstanding Paper Award and the ITC Most Significant Paper Award.



Abstract: As semiconductor technologies continue to evolve, ensuring silicon quality, reliability, and long-term health has become increasingly challenging. Modern designs require test methodologies that extend beyond manufacturing to enable continuous monitoring throughout the product lifecycle. This talk explores how advanced Design-for-Test (DFT) infrastructures provide the foundation for comprehensive silicon health monitoring, integrating on-chip intelligence, diagnostics, and lifecycle analytics to improve test quality, reduce cost, and enhance reliability from manufacturing through field deployment.

4. Semiconductor Test: A Product Perspective

Speaker: Arojit Roychowdhury (Qualcomm)

Bio: Senior Director of Technology at Qualcomm India, leading chipset engineering for Snapdragon-based mobile platforms from concept through high-volume production. He has over two decades of experience with leadership roles across SoC design, architecture, and customer engineering at Qualcomm, Texas Instruments, and Intel; he holds an M.Tech in Electronic Systems from IIT Bombay and a Bachelor's in Electronics from the University of Mumbai.



Abstract: As semiconductor products evolve from ultra-low-power edge devices to high-performance computing platforms, meeting increasingly stringent targets for power, performance, area, cost, and quality has become a defining industry challenge. Semiconductor test plays a pivotal role in bridging design and manufacturing by enabling high yield, product quality, and rapid time-to-market. This talk presents a product-centric perspective on semiconductor test, highlighting its growing importance in delivering reliable, scalable, and manufacturable silicon for high-volume production

1.A Day in the Life of a DFT Engineer – Can Agents Help?

Speaker: Jayashree Saxena (Anora Labs)
Bio: Vice President, Semiconductor DFT at Anora LLC, with over 30 years in Design-for-Test. Before joining Anora in 2013 she spent nearly 20 years at Texas Instruments. She holds an M.E. in Electrical Communication Engineering from IISc Bangalore and a Ph.D. in Electrical and Computer Engineering from the University of Massachusetts at Amherst.



2. Built-in Intelligence in Analog-to-Digital Converters

Speaker: Nithin Gopinath (Texas Instruments)
Bio: Senior Member Technical Staff at Texas Instruments, where he has spent over 15 years advancing high-speed data converter technologies. As Post-Silicon Validation & Test Manager for the High-Speed ADC group, he has deep expertise in high-speed pipelined and sigma-delta ADCs and intelligent calibration across wireless, aerospace, defense, and instrumentation applications.

Abstract:
 As modern semiconductor systems demand higher speeds, greater integration, and lower power consumption, ensuring consistent analog performance has become increasingly challenging. This keynote explores the evolution of high-speed ADC testing, from traditional trimming techniques to intelligent digital-assisted correction and real-time background calibration. It highlights how built-in intelligence is transforming analog design and test methodologies, enabling improved performance, reduced test costs, and greater resilience to process, voltage, and temperature variations.



3. System Level Test at Hyperscale: Transforming DFT for Data Infrastructure

Speaker: Nikhil Sudhakaran (Marvell)
Bio: Director of Engineering at Marvell, leading Design-for-Test for custom silicon powering next-generation AI infrastructure in hyperscale data centers, with over two decades in semiconductor design and test. Across Marvell, Intel, and Qualcomm he has delivered complex SoCs spanning client, server, mobile, IoT, and automotive, with expertise from DFT architecture through post-silicon validation and ATE bring-up.

Abstract:
 The rise of AI-driven data infrastructure is redefining the demands placed on modern semiconductor systems. As designs evolve from monolithic SoCs to heterogeneous, chiplet-based architectures featuring advanced packaging, high-bandwidth interfaces, and memory-centric computing, traditional Design-for-Test (DFT) approaches are no longer sufficient. This keynote explores how hyperscale workloads and platform-level integration are driving a shift toward system-level test strategies, highlighting the need for hierarchical, package-aware, and data-driven methodologies to ensure quality, reliability, and scalability in next-generation AI infrastructure.

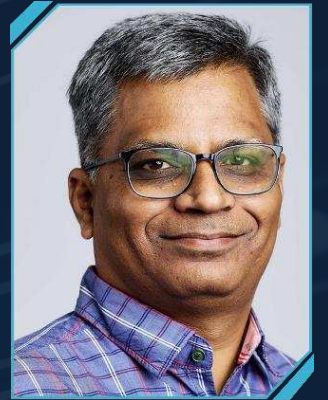


4. Testing High Speed Flash Interface I/Os

Speaker: Gopikrishna Siddula (SanDisk)

Bio: Member of the Mixed-Signal IP team at SanDisk for over 12 years, specializing in the design and integration of high-performance memory interface I/Os. He holds an M.S. from IIT Hyderabad and is an inventor on multiple U.S. patents covering high-speed I/O design, ESD protection, and memory interface technologies.

Abstract: As flash memory technologies continue to deliver higher bandwidth and lower latency, the design and validation of high-speed interface I/Os have become increasingly critical to ensuring reliable data transfer and system performance. Testing these interfaces presents unique challenges, including signal integrity, timing margins, and robustness under demanding operating conditions. This talk explores the methodologies and best practices for validating high-speed flash interface I/Os, highlighting the role of advanced test techniques in enabling reliable, high-performance memory systems for next-generation storage applications.



5. Speaker: Anand Muthaiah (Tessolve)

Bio: Senior Vice President and Head of the COE and Post Silicon Business Unit at Tessolve, with over 31 years in semiconductor testing. An expert in digital, analog, and mixed-signal test methodologies with deep experience in post-silicon validation and high-volume manufacturing, he holds an M.S. in Electrical Engineering from the University of South Florida and has held technical and leadership roles at Cyrix Semiconductor, LTX Corporation, Intel Technologies, and Tessolve.



INDUSTRY SHOWCASE

CALIBER AND TEAM

Caliber Interconnects

RESEARCH-DRIVEN SEMICONDUCTOR TEST ENGINEERING FOR SILICON INNOVATION

Abstract

The rapid evolution of semiconductor technologies, including AI accelerators, chiplet architectures, high-speed interfaces, and advanced packaging, requires innovative test engineering solutions to ensure product quality, reliability, and reduced time-to-market. This presentation highlights a research-driven approach to semiconductor test engineering that integrates Automatic Test Equipment (ATE), advanced test hardware, package design, signal and power integrity analysis, and AI-assisted automation across the silicon development lifecycle. It presents a portfolio of research covering production test optimization, post-silicon validation, intelligent fault diagnosis, scan optimization, reliability assessment, and emerging methodologies for photonics, neuromorphic, quantum, and heterogeneous semiconductor devices. The presentation also demonstrates how reusable hardware architectures, predictive analytics, and design automation enhance testing efficiency and manufacturing readiness. By combining industrial engineering expertise with applied research, the proposed framework establishes semiconductor test engineering as a key enabler of silicon innovation, delivering scalable, reliable, and cost-effective solutions for next-generation integrated circuits and advanced electronic systems.

INDUSTRY SHOWCASE

PARESH BHARKHADA

Teradyne

WAFER TO RACK. CHIP TO CLOUD. TESTED BY TERADYNE

Speaker Biography

Bio: Paresh Bharkhada is Managing Director at Teradyne, leading strategic growth and the company's expansion across India and other Emerging Markets. He established Teradyne's India presence and positioned the company for long-term success as the India Semiconductor Mission (ISM) accelerates the country's chip ecosystem, laying the groundwork for the next phase of leadership.

With over 20 years in the semiconductor industry, he previously scaled Intel's Development Cloud initiative and has been part of several industry-defining tapeouts of the most advanced chips of their time. Paresh holds an MBA from Berkeley Haas, an MS in Electrical Engineering from the University of Windsor, and a Master of Microelectronics Engineering from RMIT University, Australia.



Abstract

This presentation shows how Teradyne's solutions cover the full electronics manufacturing value chain, wafer to rack, from chip level testing through packaging, memory, board level, and system level test, to fully assembled AI data center infrastructure. It highlights the growing importance of system level test in catching real world defects that traditional test methods can miss, particularly for complex, multi die AI and compute chips. It also covers Teradyne's robotics business as a complementary growth area, supporting automation across manufacturing and logistics operations.

ADIR ZONTA

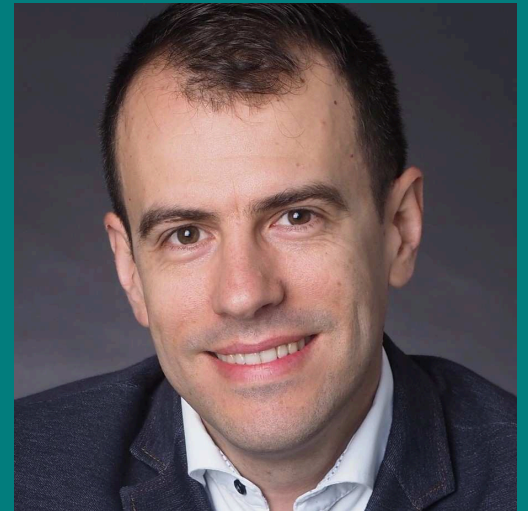
Advantest Europe GmbH

EVOLVING DFT VALIDATION METHODOLOGIES FOR COMPLEX DIGITAL DESIGNS

Speaker Biography

Adir Zonta is Product Marketing Manager for Automated Silicon Validation at Advantest, where he focuses on accelerating time-to-market and improving product quality through scalable, automated validation workflows. He collaborates closely with partners across the semiconductor ecosystem, including EDA, to deliver integrated, future-ready solutions.

With over 20 years of cross-industry experience in ecosystem development and integrated solutions, Adir brings a holistic perspective to silicon validation—spanning the entire value chain from pre-silicon test development to bench validation and ATE engineering. He is passionate about translating complex challenges into practical, forward-looking solutions that deliver measurable customer impact.



Abstract

As performance-driven digital designs continue to scale in complexity, Design-for-Test (DFT) engineering faces increasing pressure to validate test content rapidly and with high confidence. While DFT structures and patterns are defined pre-silicon, effective validation and debug are typically deferred to post-silicon environments, often relying on internally developed benches with limited observability and inconsistent alignment to downstream ATE requirements. At the same time, growing pattern volumes and increasingly complex scan architectures expose the limitations of ad hoc validation approaches, leading to inefficiencies and late-stage rework. This work introduces a structured methodology for post-silicon DFT validation, spanning controlled execution of test content, iterative debug and refinement, systematic margin exploration, and readiness preparation for production test. By emphasizing execution fidelity, observability, and workflow consistency, the approach enables earlier insight into test behavior, reduces debug cycles, and improves confidence ahead of ATE deployment. Overall, this methodology-driven validation provides a more predictable and scalable path to test readiness, supporting the demands of advanced digital designs.

HAGEN GOLLER

Advantest

SSN AND IJTAG-AWARE ATE

Speaker Biography

Speaker Biography —Hagen started his work career in 1997 and moved into Semiconductor Test in 2001. Since then, he has held various positions in Application Support, Marketing and R&D around the Advantest V93k ATE Platform. Currently he is a technical director in product marketing, looking into new test methodologies and solutions for both ATE and SLT.



Abstract

Over the past decades, scan and BIST patterns have typically been treated as a black box by most test engineers. These patterns were executed, results were retrieved and logged, and optionally, additional failure data was recorded for diagnosis and yield learning. The abundance of replicated units with spares is changing this approach. The SSN On-Chip Compare feature enables the testing of an unlimited number of units in parallel with a constant size pattern and efficiently identifies defective units that must be replaced by spares. To utilize features like on-chip compare or per-core Pass/Fail detection, semantic information about the content of the pattern is required. Specific bits of the patterns must be read or modified during test program execution. In the past, this has been achieved by adding semantic information to STIL annotations, which are converted to external csv files or pattern comments and parsed by user code. Tessent Shell and SmarTest introduce new capabilities that establish a solid foundation for handling the SSN metadata and enable convenient and efficient access to it at both the API level and in user interfaces for interactive usage and debugging. This paper explains these new capabilities and demonstrates how an end-to-end solution, including pattern translation tools, works.

PANELS

Correlation Crisis in Semiconductor Test: Can AI Bridge the Gap?

Moderator



Sameer Chillarige
Cadence, India



Udayakiran Yallamaraju
Qualcomm



John Schulze
AMD



C Jagadish Kumar
Intel



Raghu G G
Infineon

The Economics of Test: Where Should We Spend the Budget?

Moderator



Navin Bishnoi
Marvell Semiconductors,
India



Alpa Sood
Teradyne



Gowrisankar A.
Caliber Interconnects



Ruchir Dixit
Siemens



Jeff Rearick
AMD

PANELS

India's Semiconductor Test Ecosystem: Growth story and Sustainability challenges

Moderator



Gaurav Bhargava
Qualcomm, India



Jayashree Saxena
Anora Labs



Jaynarayan T. Tudu
IIT Tirupati



Dr. Rubin Parekhji
Texas Instruments



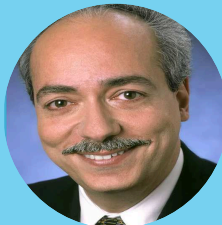
Surya Musunuri
Infineon

Scaling DFT in the era of AI, HPCs, Chiplets – Are traditional DFT approaches efficient for MCMs and Chiplets?

Moderator



Kamlesh Pandey
Krivya Semicon, India



Dr. Yervant Zorian
Synopsys



Rajesh Vaddempudi
Advantest



Dr. Shalini Pathak
STMicroelectronics



Srinivas Vooka
Google



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5. Govarthanam Krishnasamy

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6. Manoj Pachaiyan and Senthilkumar Dhamodharan

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8. Jaya Surya Moorthy, Kalyana Sundaram Chandran and Senthilkumar Dhamodharan

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- 18. Siddarth Ambhorkar, Vevekanenda Gonugunta, Ramesh Chandel, Gaurav Matthey, Daniel Tille, Aneri Jain, Naveen Kumar M, Nithin Radhakrishna Pillai and Aditya Girish**
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- 19. Meghana L, Sravan Kumar Challa, Leela Krishna Thota and Narendra Kumar Napa**
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- 20. Pervez Garg, Parth Kadiya and Pavithra K**
A Novel Test Point Insertion Methodology for Enhanced Test Efficiency and Improved Design Quality
- 21. Salome Packiavathy, Venkatesh Vandrangi, Suraj Muzhayil Chathoth and Gevorg Torjyan**
In System Test – Driven Memory Initialization for Improved Reliability in Multimode SoCs
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A Functionally Self-Testable RISC-V Processor Using a Custom Test Instruction Set

POSTER

TITLE

A Process-Aware Multi-Task U-Net Framework for Mixed Wafer Defect Localisation and Diagnosis in Semiconductor Manufacturing

Venkatesh Kanago, Yashaswini Gadad and Sujithkumar Malaghan

Abstract

The detection of wafer defects constitutes an essential component in the domain of semiconductor manufacturing, as the failure to detect or accurately analyse defects directly influences the yield efficiency and the stability of the devices produced. Despite the notable success of deep learning approaches in the classification and localisation of the wafer defects, the majority of current methods assume the existence of a singular, dominant defect pattern and provide limited interpretative outcomes for fabrication engineers. In real-world fabrication settings, wafers often display a diversity of defect patterns arising from the multiple processes variations. This work presents a process-aware, multi-task U-Net-based framework that together performs pixel-level defect localisation and multi-label classification of defects mechanisms. The proposed methodology segregates intricate wafer maps into essential base defect mechanisms and associates their combinations with 38 distinct defect classes specified in the WM-38K dataset. The model links defects to fabrication stages, improving detection accuracy. The efficacy of this approach in various defect conditions is evaluated by the WM-38K dataset, which shows improved segmentation and dependable multi-label classification. Helping the fabrication engineers make better decisions and increase yield, the model includes localisation, classification, and process awareness.

POSTER

TITLE

Bluetooth BLE FW based Test Methodology on ATE

Sai Sumanth Muppavarapu and Christina Kichenamourty

Abstract

Existing test methodology uses register setups to perform Bluetooth BT-BLE tests. In a production environment, this is exhaustive and unstable thereby posing a challenge to ship quality samples to customer. FW based approach has proven to speed up the testing process and improve the quality of the samples, including an improved yield. Usually, the FW is delivered in hex format and downloaded into BT System-RAM and executed through HCI commands using UART communication. This method is identical to the BLUETOOL followed on the bench. The UART method was noticed to be exhaustive as it runs at 119200bps, which does not aid in Test Time savings but offers stability. To counteract this issue, SWD was used to replace UART. SWD is capable of communicating at frequency in excess of 25Mhz based on device application. This approach saves almost 85% of the test time in addition to improving stability.

POSTER

TITLE

Concurrent Functional Intelligence During Structural Test Using Selective Hierarchical Core Scan Bypass in Field-Deployable SLM IP

**Hitesh Pradhan, Godithi Lakshmi, Aruna Santhi, Rohit Mate,
Sujit Panda, Vikas Gadi**

Abstract

As silicon systems evolve toward data-driven reliability and adaptive performance management, Silicon Lifecycle Management (SLM) IP must remain operational across manufacturing, validation, and in-field phases. Traditional scan methodologies, however, force functional quiescence and inject shift-induced switching activity, fundamentally constraining real-time silicon analytics.

This work introduces a selective hierarchical core scan bypass architecture that enables concurrent functional execution during structural test. The proposed micro-architectural reconfiguration dynamically partitions scan domains, suppresses shift propagation into analytics logic, and preserves complete test accessibility. Silicon validation demonstrates effective disturbance mitigation and seamless integration into existing DFT flows, establishing a scalable and non-intrusive framework for lifecycle-aware intelligent silicon.

POSTER

TITLE

Leveraging Generative Artificial Intelligence for Automated Test Equipment (ATE) Test Program Generation in Semiconductor Validation and Production

Govarthanam Krishnasamy

Abstract

Automated Test Equipment (ATE) test program development is a critical bottleneck in semiconductor post-silicon validation and high-volume manufacturing. As integrated circuits grow in complexity—driven by advanced process nodes, heterogeneous integration, mixed-signal architectures, and safety-critical requirements—the effort required to translate device specifications, datasheets, characterization reports, and validation plans into production-ready ATE test programs has increased significantly. Traditional workflows rely heavily on manual scripting, domain expertise, iterative debugging, and fragmented toolchains, resulting in extended development cycles, inconsistent test coverage, knowledge silos, and high engineering overhead.

This paper presents a comprehensive Generative Artificial Intelligence (GenAI)-driven framework for automated ATE test program generation that redefines the conventional test development lifecycle. The proposed system leverages large language models (LLMs) fine-tuned with semiconductor domain knowledge to interpret structured and unstructured inputs—including device specifications, register maps, electrical limits, timing diagrams, and test coverage matrices—and automatically generate optimized, executable ATE test code tailored to specific tester platforms. The framework integrates domain-constrained prompt engineering, retrieval-augmented generation (RAG), rule-based constraint validation, and coverage-aware reasoning to ensure functional correctness, electrical compliance, and traceability to requirements.

In addition to script generation, the architecture incorporates intelligent modules for test flow optimization, binning logic generation, parametric limit extraction, corner case identification, and reusable test template synthesis. An embedded verification layer performs syntax validation, static analysis, and rule compliance checks to minimize runtime failures on tester hardware. Furthermore, feedback loops from silicon debug data and production yield analytics enable continuous learning and adaptive refinement of generated test programs, forming a closed-loop TestOps ecosystem.

Experimental evaluations across mixed-signal and digital device case studies demonstrate substantial reductions in ATE program development time, improved test coverage consistency, faster debug cycles, and enhanced cross-team collaboration. The results indicate that GenAI-driven ATE automation not only accelerates time-to-market but also standardizes test quality, preserves institutional knowledge, and scales efficiently across device families and tester platforms. The proposed approach establishes a foundational paradigm for AI-assisted semiconductor test engineering, paving the way for autonomous, self-optimizing test program generation in next-generation manufacturing environments.

POSTER

TITLE

DRAC: A Dynamic Reconfigurable ATE Core for Extending Tester Capability in High-Resolution Data Converter Testing

Manoj Pachaiyan, Senthilkumar Dhamodharan

Abstract

The proliferation of ultra-high-resolution data converters (20–24 bits, >110 dB dynamic range) has created a critical capability gap in semiconductor high-volume manufacturing (HVM), where device performance increasingly exceeds the maximum capability of production Automatic Test Equipment (ATE). Contemporary platforms such as Advantest Wave Scale MX and Teradyne μ PAC employ internal stimulus generators with approximately 16-bit effective resolution, resulting in measurement chains that underestimate analog-to-digital converter (ADC) performance by 10–15 dB due to residual noise and harmonic distortion. Although laboratory-grade bench instruments provide adequate stimulus purity, they lack the automation, scalability and throughput required for production environments. Consequently, existing approaches struggle to extend ATE measurement capability while maintaining manufacturing efficiency.

This work introduces DRAC (Dynamic Reconfigurable ATE Core), a synchronized hybrid architecture that integrates ultra-low-distortion external stimulus sources (>130 dB SFDR) with production ATE capture engines through deterministic clock distribution. DRAC dynamically reconfigures the measurement chain based on device-under-test specifications while preserving native ATE automation.

The key contributions include: (1) a measurement-chain-aware analytical framework that quantifies the interaction between stimulus spectral purity, timing stability, capture resolution, and FFT-based spectral processing; (2) systematic reconfiguration protocols guaranteeing controlled dynamic margins greater than 15 dB across stimulus-DUT-capture subsystems; and (3) coherent sampling enforcement that eliminates spectral leakage during FFT-based dynamic evaluation. Experimental validation across precision ADC architectures demonstrates more than 10 dB SNR recovery, 1.8–2.2 bit ENOB improvement and SFDR enhancement from 95 dB to 118 dB relative to conventional internal ATE stimulus methods. DRAC enables laboratory-grade dynamic characterization within production ATE environments with less than 5% throughput impact, providing a scalable and forward-compatible validation framework for next-generation high-resolution data converters. Future extensions of multi-channel testing are also discussed at the end of the paper.

POSTER

TITLE

ATE-AMFE: Automated Multi-Platform Feasibility Engine

Venkatraman Sivagnanam, Naveena Natarajan, Jaikrishnan Balakrishnan,
Senthilkumar Dhamodharan

Abstract

The increasing complexity of semiconductor devices and the use of multiple Automatic Test Equipment (ATE) platforms in modern manufacturing environments have significantly increased the challenges associated with efficient test program deployment. Semiconductor test facilities commonly operate heterogeneous tester platforms such as Advantest V93K, Teradyne UltraFLEX, J750, and ETS, each offering different hardware resources, instrument capabilities, and operational constraints. Determining whether a device test program can be executed on a specific tester platform typically requires manual feasibility analysis performed by experienced test engineers.

This conventional approach presents several challenges, including significant engineering effort, inconsistent decision-making, and potential configuration errors resulting from complex dependencies among tester resources such as channel availability, timing resources, voltage and current limits, instrument ganging, synchronization modules, and licensing constraints.

These limitations can delay test program deployment and reduce overall tester utilization efficiency. To address these challenges, this paper proposes ATE-AMFE, an Automated Multi-ATE Platform Feasibility and Optimization Framework that systematically evaluates device test requirements against multiple tester platform capabilities.

The proposed methodology integrates a structured tester capability database with a rule-based resource mapping and constraint evaluation engine to analyze parameters such as operating frequency, voltage range, current requirements, timing accuracy, and channel count. Experimental evaluation demonstrates that the proposed framework reduces feasibility analysis time by approximately 75–80%, improves platform selection accuracy to over 94%, and significantly minimizes configuration errors. Future work will focus on integrating machine learning techniques for predictive tester resource allocation and intelligent test program deployment, enabling more adaptive and efficient semiconductor test planning.

POSTER

TITLE

Data-Driven Post-Silicon Validation Framework for High Bandwidth Memory in 2.5D Integration: Adaptive Stress Testing and Hierarchical Fault Isolation

Jaya Surya Moorthy, Kalyana Sundaram Chandran, Senthilkumar Dhamodharan

Abstract

High Bandwidth Memory (HBM) has emerged as a critical enabler for high-performance computing, artificial intelligence, and graphics processing applications, offering unprecedented memory bandwidth through 3D-stacked DRAM integrated via 2.5D silicon interposer technology. However, the complex multi-die architecture, involving through-silicon vias (TSVs), microbump interconnects, and high-speed serial interfaces, presents significant post-silicon validation challenges.

This paper presents a comprehensive data-driven post-silicon validation framework specifically designed for HBM subsystems in 2.5D packages. The proposed methodology integrates adaptive stress-based traffic generation, automated shmoo-based multi-dimensional margin analysis, lane-level skew profiling, hierarchical fault isolation mechanisms, real-time telemetry-assisted monitoring, and correlation-aware debug analytics. Silicon validation results from a production HBM2E subsystem demonstrate a 35% reduction in debug turnaround time, 28% improvement in timing margin visibility, 22% enhancement in defect localization efficiency, and 30% reduction in manual intervention compared to conventional approaches.

POSTER

TITLE

Enabling Robust IEEE 1687 Interoperability in Heterogeneous IJTAG Networks through SIB Adaptor Architectures

Vistrita Tyagi, Kshitij Kulshreshtha, Amihay Rabenu,
Manish Arora

Abstract

Modern SoCs often integrate IEEE 1687 (IJTAG) components sourced from multiple vendors, revealing understated but significant differences in Capture/Shift/Update (CSU) semantics: most notably one-hot (C_S_U) versus non-one-hot (CS_U; capture remains asserted during shift). These mismatches complicate ICL/PDL handling, pattern generation, and test-cycle QoR, particularly when attempting to operate mixed networks under a single TAP. We introduced an adaptive SIB Architecture that performs bidirectional CSU translation, enabling heterogeneous IJTAG networks to interoperate under one TAP without modifying customer RTL.

The approach comprises: (i) enhanced SIB/TDR (segment insertion bit, test data register) hardware that deterministically translates Shift/Capture behavior within a single interface; (ii) ICL schema extensions with attribute propagation to encode function modifier semantics; and (iii) automation for ICL/PDL generation with PDL solver compatibility. Practically, one SIB flavour converts (C_S_U $\rightarrow$ CS_U) to normalize behavior across lower-level hierarchies, while a complementary flavour converts (C_S_U $\rightarrow$ CS_U) at the top of the hierarchy to align with TAP expectations. Evaluations on representative hierarchies demonstrate correct ICL extraction, conflict-free attribute resolution, and accurate PDL execution across mixed networks.

The solution eliminates separate test partitions, simplifies integration with networks requiring inconsistent signaling, and improves end-to-end test efficiency, while informing prospective 1687.x harmonization of CSU representations and cross-vendor interoperability. Results show that the adapter-based translation approach eliminates the need to maintain separate test networks, reduces vector generation complexity, and delivers measurable improvements in end-to-end test cycle reduction.

The work further provides insights for future IEEE 1687.x standardization efforts, especially around harmonizing CSU representations, and cross-vendor interoperability mechanisms.

POSTER

TITLE

Virtual Emulation Ecosystem for Rapid Pre Silicon Validation

V N Sivakumar Avvaru, Srinivasan Arulanandam, Harini Sriram

Abstract

Achieving first time right silicon is critical for ensuring product quality, sustaining market leadership, and meeting aggressive time to market objectives. This requires comprehensive pre silicon validation capable of identifying all non recoverable defects prior to tape in (TI). However, traditional In Circuit Emulator (ICE)–based validation environments are no longer viable due to limited availability, high cost, operational instability caused by extensive physical connectivity, and restricted debug visibility.

As system on chip (SoC) complexity continues to grow, these limitations significantly slow verification closure and delay silicon readiness. This work presents a virtual emulation–based validation framework that replaces physical dependencies with virtual interfaces, soft peripheral models, protocol aware monitors, and intelligent, event driven waveform capture.

The proposed approach improves stability, scalability, determinism, and debug efficiency, enabling earlier detection of system level defects. In addition to technical benefits, the framework delivers tangible business impact by reducing reliance on scarce ICE infrastructure, improving engineering productivity, and preventing costly post silicon re-spins.

Based on conservative industry assumptions, the approach yields an estimated USD 4–5 million cost savings per SoC project, primarily through productivity gains and avoidance of at least one silicon re-spin. The results demonstrate that virtual emulation is an effective and economically compelling strategy for achieving predictable and successful first pass silicon.

POSTER

TITLE

A Shift-Left Framework for Automated RTL-Level Correction of Testability Violations to Improve Stuck-At and Transition Fault Coverage

Sunny Kumar, Yeturi Om Sasankar, Philemon Daniel

Abstract

—In VLSI design flow, Design-for-Testability violations are identified only after synthesis, forcing costly manual RTL rework and design iterations. This paper presents an automated shift-left framework that detects circuit-dependent conditions like combinational loops, gated clocks, asynchronous resets and redundant logic that results in decrease of Stuck At Fault and Transition Fault coverage, directly at RTL stage.

The framework generates corrected Verilog through source-to source transformation by preserving functional equivalence, and quantitatively validates improvement using ATPG-based fault coverage analysis and static timing analysis. By closing the detect fix-validate loop prior to synthesis, this approach allows designers to enter the synthesis phase with testability-clean RTL.

POSTER

TITLE

Smart Test Line Selection for Pre- and Post-Silicon Validation: Leveraging AI for Enhanced Efficiency

Ashwani Kumar, Trupti Joshi, Vishal B
Bhogade, Hemanthkumar Sivaraj

Abstract

Pre-silicon verification and post-silicon validation of complex SoC and processor designs face a test content explosion: the number of functional test scenarios required to achieve thorough coverage has grown dramatically with each generation, leading to unsustainable validation time and cost. This paper presents a novel AI-driven methodology that intelligently reduces redundant test lines while maintaining near-complete coverage.

We leverage hardware performance counter data collected from test executions to identify groups of tests exercising similar behaviors. By applying machine learning—including robust data preprocessing, feature selection, t-SNE visualization, and K-Means clustering with outlier analysis—our approach selects a minimal representative subset of tests.

We evaluate the method on two real Intel CPU validation suites: a 1212-test mesh network traffic suite on a high-core-count server platform (Intel Granite Rapids/Sierra Forest, GNR/SRF) and a 363-test memory coherency suite on the same system.

The results show a 67% reduction in test count for the mesh suite (1212 to 394 tests) and 40% reduction for the memory suite (363 to 216 tests), while preserving approximately 95% of the coverage of the full suites. We validate that the pruned suites retain the bug-finding capabilities and corner-case coverage of the originals using fault injection and functional coverage analysis.

We also compare against baseline test-reduction strategies (random pruning and greedy coverage-based selection) and find that our method achieves higher coverage with significantly fewer tests. An ablation study quantifies the contribution of each pipeline component (robust scaling, variance filtering, outlier retention) to performance. These contributions enable more efficient validation flows, addressing a critical bottleneck in modern hardware development.

POSTER

TITLE

Scalable Fanin-Fanout Analysis Using Precomputed Reconvergence Data for DFT Verification

Tushar Jeevan, Chandan Kumar, Meetu Agarwal, Suraj Kashyap

Abstract

BIST methodologies require accurate identification of high fanin-fanout logic to ensure testability and pattern generation quality. Precise fanin-fanout counting is critical for validating design constraints, but reconvergent logic structures cause path over-counting, leading to false violations. Direct reconvergence-aware counting during traversal incurs prohibitive runtime on large designs.

This paper presents a novel two-phase approach: first, a preprocessing algorithm identifies all reconvergence points circuit-wide. Subsequently, gate input and fanout limit validation rules leverage this precomputed data to correct counts accurately without redundant analysis. Our parallelized implementation eliminates false positives while achieving scalable performance on industrial designs.

POSTER

TITLE

A Cache-Resident Linux Framework for System-Level Validation on Enterprise-Class Processors

**Manish Mukul, Madhavan Srinivasan, Mahesh
Salgaonkar, Aditya Gupta**

Abstract

This work presents a novel framework for running a fully functional Linux environment entirely within the on-chip processor-cache hierarchy of an enterprise-class processor with no external DRAM, storage or I/O attachments.

The framework uses a deterministic cache-as-RAM model and a carefully controlled memory layout to preload and retain the Linux kernel, root-filesystem and runtime workloads exclusively in caches ensuring zero cache misses throughout execution.

By reshaping kernel memory assumptions and constraining the working set to a bounded cache footprint, the system provides a complete, self-contained Linux instance capable of supporting complex validation workloads using only on-chip resources.

POSTER

TITLE

HBM - Case study on a modern complex SOC with multi-die

Padmini Prakash and Pradip Kapure

Abstract

As Machine Learning (ML) workloads push the boundaries of modern Systems-on-Chip (SoCs), the integration of High Bandwidth Memory (HBM) via high-density interposers has become an architectural necessity. However, testing these advanced heterogeneous packages introduces significant complexity.

This paper discusses the Design for Test (DfT) strategies utilized in modern HBM integration, evaluating both the capabilities of current testing frameworks and the specific limitations that arise when ensuring the reliability of high-density substrate interconnects.

POSTER

TITLE

A Weighted Hierarchical Approach to Testpoint Configuration driving Efficient and Optimized DFT Convergence

Krunal Siddhapathak, Tathagat Biswas

Abstract

As System-on-Chip (SoC) complexity scales, traditional "brute force" Design-for-Test (DFT) methodologies face significant challenges in balancing high test coverage with stringent Physical Design (PD) constraints. Conventional Testpoint Insertion (TPI) often applies a uniform distribution across the floorplan, leading to pattern count inflation and timing closure bottlenecks in Place and Route (PnR).

This paper proposes a granular, hierarchical TPI methodology utilizing EDA tools to optimize testability in high-complexity designs. The core of the proposed approach is a multi-pass, "no-faulting" analytical flow that identifies specific hierarchical blocks—"testability black holes"—contributing disproportionately to Automatic Test Pattern Generation (ATPG) overhead. By shifting from a monolithic distribution to an iterative, targeted refinement strategy, testpoints are strategically placed only within ATPG-critical hierarchies.

This method ensures that high fault coverage is achieved without compromising the design's physical integrity or Static Timing Analysis (STA) targets. Experimental results demonstrate that this hierarchical targeting significantly reduces pattern counts and total test time compared to traditional TPI. Furthermore, the reduction in global testpoint density facilitates a streamlined path through PNR, delivering a superior Quality of Results (QoR) while maintaining predictive control over silicon quality.

POSTER

TITLE

Protection of PUF Architectures Against Machine Learning Attacks Using Differential Privacy

Ravi Bandla, Venkata Sreekanth Balijabudda

Abstract

Physical Unclonable Functions (PUF) are widely used as lightweight hardware security primitives. However, advances in Machine Learning (ML) have made delay-based PUFs vulnerable to model-building attacks, particularly with large-scale challenge–response pair (CRP) datasets.

This work investigates an adaptive defense mechanism inspired by Differential Privacy (DP) to mitigate ML-based PUF modeling attacks. For each PUF, two million CRPs are generated and transformed into logistic regression–style feature vectors, after which Gaussian noise is injected that is calibrated from differential privacy parameters.

The robustness of the perturbed datasets is evaluated against state-of-the-art ML-based attacks. Experimental results indicate that our technique exhibits considerable resistance to model-building of Arbiter, XOR Arbiter, and Interpose PUFs.

POSTER

TITLE

Detecting Crosstalk-Induced Static Noise Defects Using a Customized ATPG Test Flow

**Siddarth Ambhorkar, Vevekanenda Gonugunta, Ramesh Chandel,
Gaurav Matthey, Daniel Tille, Aneri Jain, Naveen Kumar M,
Nithin Radhakrishna Pillai, Aditya Girish**

Abstract

Modern System-on-Chips (SoCs) are susceptible to asynchronous interface failures, particularly in advanced technology nodes where crosstalk can induce voltage glitches, leading to critical post-silicon defects and possible test escapes. This paper details the investigation of a defect in an asynchronous interface that was undetectable by standard structural ATPG patterns (stuck-at, transition, path delay and bridging). Faults residing within asynchronous interfaces frequently evade detection by standard structural testing methodologies, as the associated clock domains lack a fixed frequency or phase relationship.

Functional, software testing identified read/write failures spanning two asynchronous clock domains, which persisted even during static data reads.

These observations supported the hypothesis that crosstalk might be interfering with the read path, causing a glitch to be captured at the moment of failure. Further analysis, including silicon debug, revealed a noise violation, manifesting as a glitch at an asynchronous path.

The failure mechanism was isolated to crosstalk occurring when simultaneous write operations impacted the read path with specific write values. There was a need to recreate this failing condition in the test environment. Targeted ATPG tests were generated utilizing a User-Defined Fault Model (UDFM) with the ATPG tool.

This paper explores two distinct methodologies: one involving manual netlist modifications paired with constraining scan elements to specific values to achieve the required functional fail condition and a second approach leveraging the UDFM technique. By facilitating the definition of aggressor-victim conditions in an efficient and straightforward manner, UDFM provides the necessary flexibility to replicate specific functional test requirements. The UDFM-based patterns were used to screen defective silicon parts and achieve the same response as functional tests.

POSTER

TITLE

Navigating the Intricacies of Clock Domain Crossing: The Role of Unified Power Format

**Meghana L, Sravan Kumar Challa, Leela Krishna
Thota , Narendra Kumar Napa**

Abstract

Current integrated circuits (ICs) incorporate millions of gates and numerous IPs that interface through multiple asynchronous clock domains. Ensuring the correctness of these asynchronous communications necessitates exhaustive Clock Domain Crossing (CDC) structural verification. This verification aims to detect all possible CDC paths within a design, requiring all clocks to be meticulously defined and concurrently propagated.

This verification process requires a Unified Power Format (UPF) file in which low-power components introduce new challenges and complexities. Ignoring and overlooking significant domain-crossing issues potentially compromises the design's integrity. Hence, to tackle this complexity, we proposed a VCLP tool-based novel methodology.

This tool eases the verification process by providing custom features and elaboration of additional information to designers. By adopting this proposed methodology, 32 missing LS strategies have been identified effectively in our adopted low-power design, ensuring that all asynchronous communications are correctly handled even in the presence of low-power components.

The observed results demonstrate that the proposed methodology enhances the Quality of Results (QoR) compared to the native platform by integrating UPF into the CDC verification process, thus significantly improving the robustness and reliability of modern IC designs.

POSTER

TITLE

A Novel Test Point Insertion Methodology for Enhanced Test Efficiency and Improved Design Quality

Pervez Garg, Parth Kadiya,
Pavithra K

Abstract

In today's competitive semiconductor market, optimizing device test cost while maintaining stringent quality metrics (DPPM) is paramount for market success. While Automatic Test Pattern Generation (ATPG) remains the gold standard for structural testing and failure diagnosis, achieving optimal scan coverage in complex, high-gate-count devices presents significant challenges, often resulting in bloated pattern counts and extended test times. Traditional Random Resistant Fault Analysis (RRFA) based Test Point Insertion (TPI) effectively addresses these challenges by enhancing scan coverage while reducing pattern count. However, the substantial Design-for-Test (DFT) area overhead associated with conventional TPI implementation often renders it impractical for area-critical designs.

This paper introduces a unique approach: a novel functionality-aware, timing-aware and physical-aware TPI methodology that strategically repurposes existing functional and DFT flip-flops as test points. Our comprehensive evaluation across multiple sub-chip implementations demonstrates significant improvements in both test quality and test time efficiency.

The proposed methodology effectively overcomes the traditional TPI limitations by eliminating additional area overhead, mitigating routing congestion, and minimizing leakage power - critical concerns in contemporary semiconductor design.

POSTER

TITLE

In System Test – Driven Memory Initialization for Improved Reliability in Multimode SoCs

**Salome Packiavathy, Venkatesh Vandrangi,
Suraj Muzhayil
Chathoth, Gevorg Torjyan**

Abstract

This work presents a production-proven memory reset, test, and repair methodology for a multimode, memory-intensive system-on-chip (SoC) using Tessent In-System Test (IST). Deterministic memory initialization to all zero values and early fault screening are achieved during power-up through ROM-based IST pattern execution, followed by automated repair prior to mission-mode entry.

The architecture supports dual-port and four-port operating modes without impacting functional access or timing closure. Silicon validation on a full SoC confirms correct memory initialization, successful repair of manufacturing defects, and elimination of spurious error-correcting code (ECC) errors caused by uninitialized reads, ensuring predictable system bring-up

POSTER

TITLE

An FPGA-Coordinated Validation Framework for Digital DUTs with DC and Protocol Testing for First Silicon Bring Up

Senthilkumar Dhamodharan, Sreeram V.R., Dyaneswaran Anguraj, Swetha Kumar, Shahana Balamurugan

Abstract

Structural level post-silicon validation using FPGA platforms covering MBIST, stuck-at, and transition fault models has been widely explored in prior work. However, first-silicon qualification demands broader validation coverage, including core supply current measurement and input leakage current testing, which are typically not addressed in conventional FPGA based approaches. This paper proposes a systematic extension of an FPGA based validation framework to incorporate DC test capabilities such as core supply current and input leakage measurements within a unified platform.

The system is implemented using the Opal Kelly XEM7310 featuring an Xilinx Artix-7, interfaced with a custom DUT evaluation board. External ADC/DAC based circuits are utilized for accurate voltage forcing and precise measurement of voltage and current across multiple power domains.

The proposed framework emphasizes deterministic timing, measurement accuracy, and simplified test architecture, enabling reliable DC and protocol-level validation. It also integrates SPI and I²C protocol verification, along with clock integrity checks, ensuring comprehensive functional validation.

The FPGA orchestrates all test sequences through the FrontPanel SDK, enabling synchronized control and real-time data acquisition via SPI and I²C interfaces. Experimental results demonstrate that our development system achieves approximately 65% reduction in first-silicon qualification time compared to conventional manual bench testing. This makes it a cost-effective and scalable alternative to traditional ATE, particularly for in-house bring-up and validation of SoCs and digital DUTs.

POSTER

TITLE

Pattern Count Optimization and Test Cost Reduction Using TSO.ai for ATPG

Jai Sehgal, Aditi Bahuguna, Peeyush Bhatnagar, Sruthi Nanduru, Theo Toulas, Prakyath Madadi

Abstract

Reducing ATPG pattern count is a key lever to minimize Automated Test Equipment (ATE) test time and test cost, especially in high volume semiconductor manufacturing. Traditional ATPG flows expose many interdependent parameters that are difficult to tune manually. Achieving maximum coverage with minimal patterns typically requires numerous iterations, significant engineering time, and can still result in conservative, pattern heavy solutions. Conventional ATPG can produce very large pattern sets, leading to long ATE test times and high-test cost.

To mitigate this, we adopted TSO.ai, an AI driven optimization engine that automatically learns design specific ATPG recipes, maintaining high structural fault coverage while significantly reducing pattern volume. Using a permutation based machine learning approach, TSO.ai systematically explores and refines ATPG parameters based on coverage and pattern count feedback, converging to a compact, high quality pattern set with minimal manual effort.

The case study demonstrates that AI-assisted optimization using TSO.ai can systematically reduce ATPG pattern count up to 50% on real SoC designs without compromising fault coverage or simulation quality. The proposed methodology offers a commercially viable path to lower ATE runtime and tester cost with minimal changes to existing DFT and ATPG methodologies, and provides a strong foundation for broader deployment of AI driven optimization in VLSI test flows.

POSTER

TITLE

A Functionally Self-Testable RISC-V Processor Using a Custom Test Instruction Set

Satyam Kuar, Jaynarayan T Tudu

Abstract

Ensuring reliable processor operation is critical in modern computing systems, especially in scenarios where faults may arise during runtime. Traditional approaches such as Built-In Self-Test (BIST) and Software-Based Self-Test (SBST) either incur significant hardware overhead or lack flexibility for dynamic testing.

This work presents a self-test capable RISC-V processor that enables on-demand functional validation using a lightweight architecture. A custom instruction is introduced to trigger test mode, allowing ATPG-generated test patterns stored in memory to be executed through the native datapath. A dedicated control FSM coordinates test execution, while a comparator and pass/fail counters provide efficient result evaluation.

The design ensures non-intrusive operation through a program counter save and restore mechanism, preserving the processor state during testing. Experimental validation on a single-cycle RISC-V processor demonstrates effective fault detection with minimal hardware overhead. The proposed approach is scalable and suitable for in-field testing of processor-based systems.



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